

BW 2

TECHNICAL SERVICE MANUAL

PREFACE

Objective

This technical manual describes the maintenance, troubleshooting and operating principle of the Bondwell 2 portable lap size personal computer.

Federal Communication Commission Radio Frequency Interference statement:

Warning: This equipment has been certified to, comply with the limits for a Class A computing device, pursuant to Subpart J of Part 15 of FCC rules. Only peripherals (computer input/output devices, terminals, printers, etc.) certified to comply with Class A limits may be attached to this computer. Operation with non-certified peripherals is likely to result in interference to radio and TV reception.

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The information in this manual is intended for service technicians who are required to carry out subassembly troubleshooting; and for interested parties who need to understand the design and operation of the Bondwell 2 lap size.

When performing adjustments and troubleshooting, the following documentation should be available in addition to this manual.

1) BONDWELL 2 USER'S MANUAL

- Target audience : end user (service technician should be familiar with the use of the BW2)

2) TEAC FD-35 MICRO FLOPPY DISK DRIVE MAINTENANCE MANUAL

- Target audience : service technician performing adjustments and troubleshooting on the TEAC Single Side/Double Density micro-floppy disk drive.

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CHAPTER 1 SYSTEM OVERVIEW

1.1 INTRODUCTION

The Bondwell 2 is a standalone lap size portable computer taken all the advantage of its predecessor, the BW12/14 series, but being much smaller in size. Making use of the compact size (640 x 200 dots) LCD display and the 3 1/2 in microfloppy disk drive allowing the concept of the BW2 becoming a reality.

All the essential feature of any advance computer can be found on the BW2. Not only it consists of the LCD module and the 360 micro-floppy disk drive as mentioned above. The keyboard is located on the main unit, a built-in rechargeable battery allowing continuous operation up to eight hours without mains supply, a RS232 serial interface port, one external disk drive interface port, one parallel printer interface port and a gold-finger expansion slot located on the bottom of the computer allowing cartridge-based peripherals to be added to further enhancing the BW2.

1.2 SYSTEM BOARD

The main system PCB is located horizontally on the left hand part of the base unit. It consists of the vital functional area such as :

CPU, I/O logic, BOOT ROM, RAM, VRAM, I/O ports etc.

The BW2 utilize the Z80L as its CPU which operates on 2 MHz.

The BOOT ROM is a 4K bytes 2732. It contains the cold start loader, self test routine and character generating pattern.

The BW2 uses 8 dynamic RAM 4164 which operates on 200ns.

The system board contains all circuitry for interfacing external I/O devices. The following I/O Map gives the corresponding address for accessing a particular I/O device.

PORT MAP

00H : PPI (82c55) port A
01H : PPI (82c55) port B
02H : PPI (82c55) port C
03H : PPI (82c55) control reg.
10H : TIMER (82c53) counter reg. 0 TX RX USART
11H : TIMER (82c53) counter reg. 1 LCD-Contv.
12H : TIMER (82c53) counter reg. 2 MTRON
13H : TIMER (82c53) control reg.
20H : LCD CONTROLLER data reg.
21H : LCD CONTROLLER instruction reg.
40H : USART (Serial I/O) (82c51) data reg.
41H : USART (Serial I/O) (82c51) control/status reg.
50H : Printer output port
60H : Floppy disk controller command/status reg.
61H : Floppy disk controller track reg.
62H : Floppy disk controller sector reg.
63H : Floppy disk controller data reg.

Fig. 1.1 Ports and Memory Maps

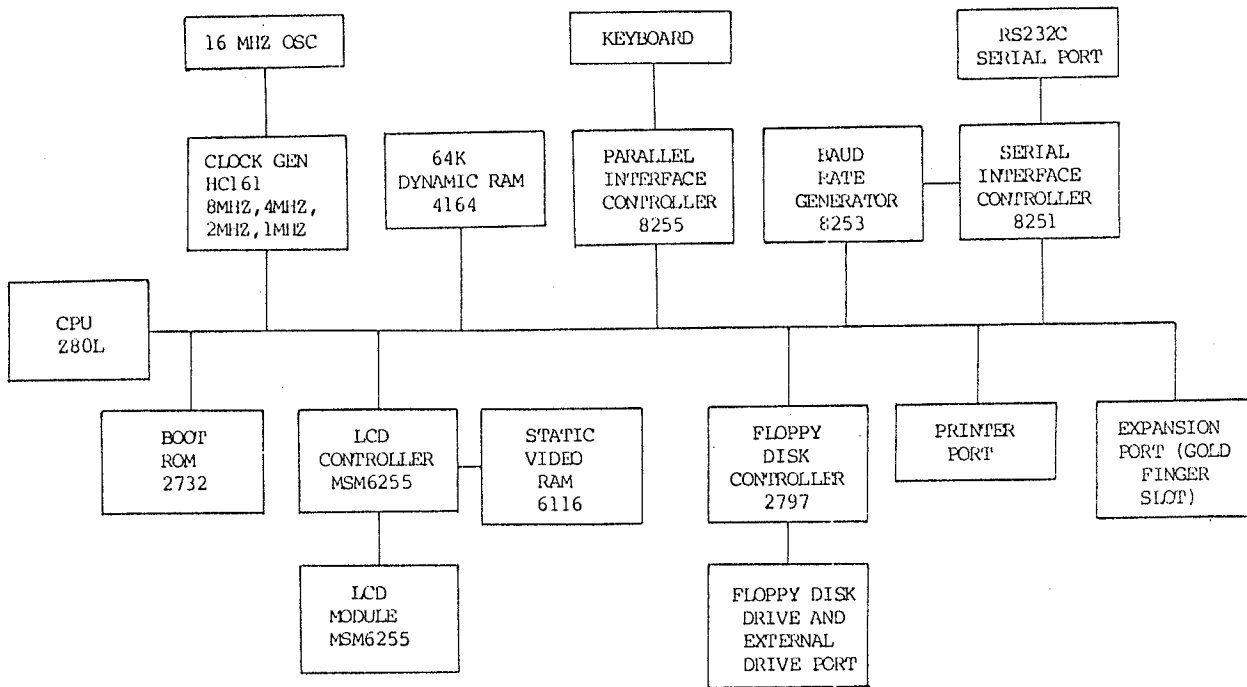
1.3 POWER BOARD

The power unit of the BW2 is situated on the rear right hand side of the base / unit. It contains a rechargeable LEAD ACID battery and a power board. The power board is placed vertically adjacent to the battery for better cooling purpose.

The power board consists of switching circuitaries to convert the +12V battery to +5V and -13.0V output for the main board and LDC module respectively while the regulated +12V is supplied to the microfloppy disk drive.

2.1 INTRODUCTION

In this chapter, you will find detail circuit description of the BW2. Read through the chapter before going to repair/service the BW2.



Bondwell 2 Functional Block Diagram

2.2 CIRCUIT DESCRIPTION

2.2.1 CENTRAL PROCESSING UNIT (CPU)

The BW2 uses the Zilog Z80L low power CMOS microprocessor ICI as its CPU. The Z80L is an 8-bits microprocessor having 16 address lines, various clock and control lines.

It operates on 2MHz signal from the clock divider IC26. The RST (PIRESET) signal comes from the power board and upon this signal the CPU resets and clears all P.C. register and restarts at location 0000H. All the address and data buses of the CPU are directly connected to the memory and I/O devices.

The $\overline{\text{WAIT}}$ input is pulled high disabling its function because the 64K dynamic RAM on-board main memory needs no wait state. The $\overline{\text{BUSREQ}}$ is also pulled high to disable because there is no need to set the various address, data and system control lines to high impedance state as there is no other bus master in the system (external device which the BW2 operates on). The $\overline{\text{BUSACK}}$ has no connection to any devices and is always found to be in a high state because $\overline{\text{BUSREQ}}$ being high constantly.

The major control signals of the Z80L are the interrupts, halt, I/O request, memory request, read/write and clock lines.

When the FDC, DWG A5, requests for data transfer. The CPU HALT goes low to enable NMI, the CPU is interrupted to allow specific function routine to be performed.

The system control buses, $\overline{\text{MI}}$, $\overline{\text{IORQ}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ is connected to the I/O logic (DWG A2) for the selection of the various I/O devices and enabling Read/Write operation to and from the system memory.

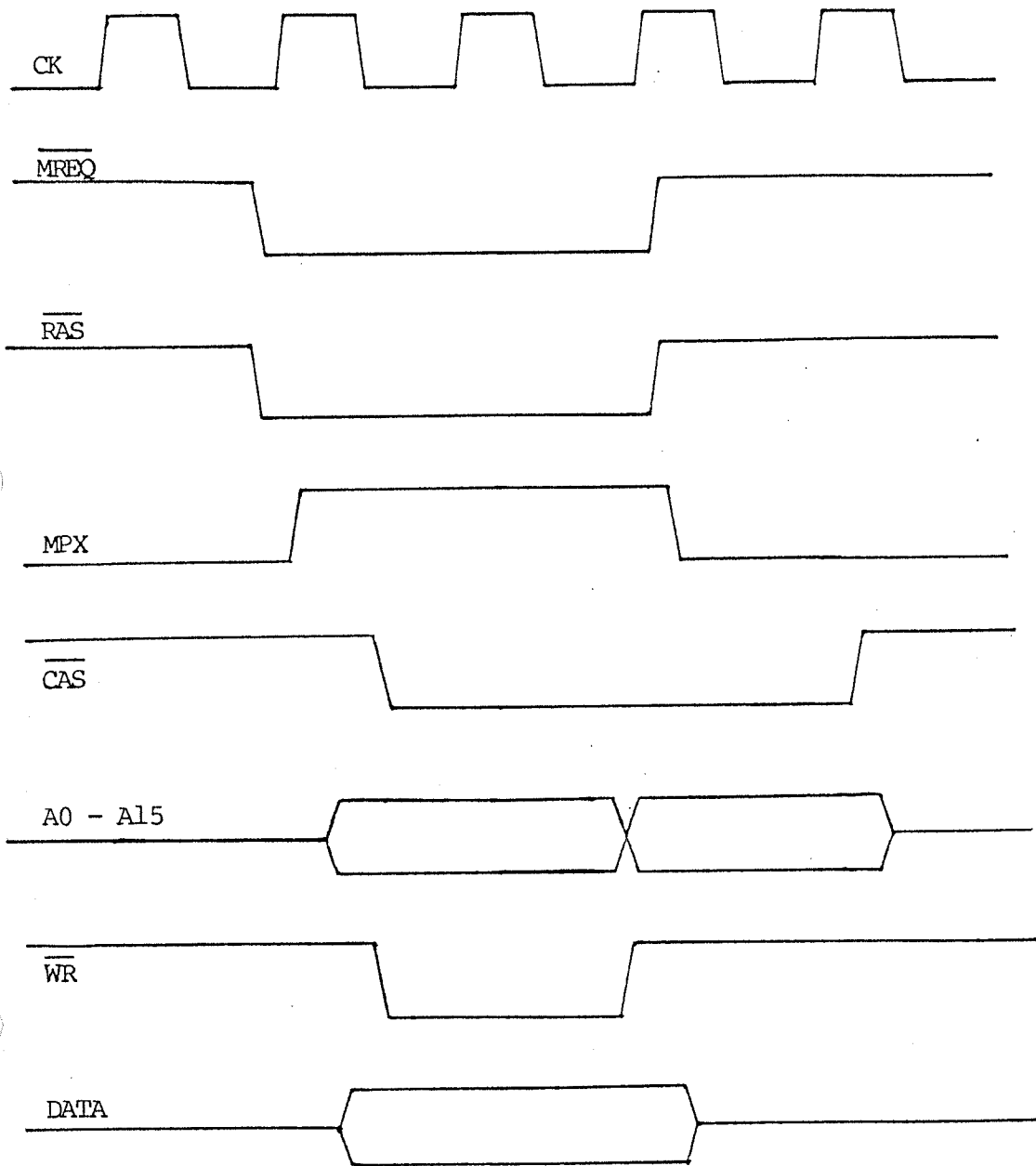


Fig. 2.1 Memory Request Timing Diagram

2.2.2 BIOS ROM

The BIOS ROM (BOOT ROM), IC8 DWG A1, is a 4K Bytes 450ns 2732 EPROM containing both the diagnostic and initialization program.

The lower 2K addresses store the cold start loader for the system while the upper 2K addresses contain the character pattern generator.

The output enable \overline{OE} and chip enable \overline{CE} is connected together and \overline{ROM} is selected by the bank selector HC138 (IC58 DWG A5) following the power-up routine and for character generation. The advantage of connecting \overline{OE} and \overline{CE} is that current consumption of the 2732 ROM is dropped to standby mode when it is not operating.

2.2.3 POWER-UP INITIALIZATION

Fig 2.2 shows the power up initialization sequence.

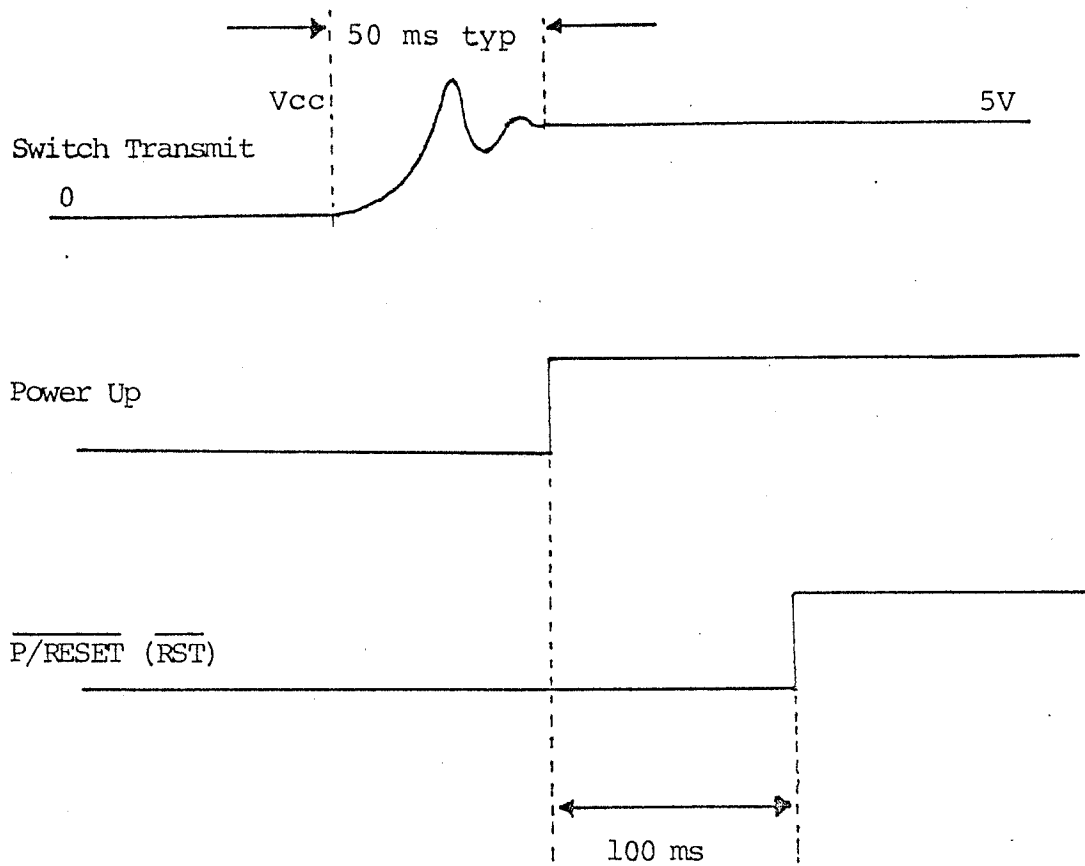


Fig. 2.2 Power Up Sequence

2.2.4 REFRESH & I/O LOGIC

The logic ICs used in the BW2 are mostly high speed CMOS. The reason of using them is mainly their low current consumption feature.

The signal provided to the dynamic RAM (main memory) is the Row Address Select \overline{RAS} , the Column Address Select \overline{CAS} and the address Multiplex MPX.

The \overline{RAS} is equal to the \overline{MREQ} from the CPU. The \overline{RAS} and MPX is made to synchronize with the CPU clock using two flip-flops 74HC74, IC28. MPX changes from low to high when it is triggered by the rising edge of t2 in a memory fetch cycle while \overline{CAS} changes from high to low when triggered by the falling edge of t2.

In order to tailor for the timing of Z80 to match those of the BW2 family I/O chips, the falling edge of the \overline{RD} and \overline{WR} is delayed to generate \overline{IORD} and \overline{IOWR} respectively. Moreover, the chip select of each chip is generated by delaying the rising edge of the \overline{IORQ} . All these are made synchronous with the CPU clock by using two D-type flip-flops 74HC74 (IC29).

Also, in the BW2, the address decoder 74HC138 (IC23, DWG A2) provides individual address selection of the peripheral I/O devices. The system can gain access to the I/O devices by calling their corresponding addresses as shown in Fig 1.1, the port and memory map. The address decoder is enable by a low on \overline{IORQ} and low on the address line A7.

2.2.5 DYNAMIC RAM

The 64K bytes dynamic RAM is built-up of eight 4164 (200ns). The upper 32K bytes bank (8000H to FFFFH) belongs to the common bank while the lower 32K bytes bank (0000H to 7FFFH) belongs to the switched bank. There are altogether eight switched banks, Fig. 2.4 Memory Map, controlled by the bank decoder (IC58 HC138). In these eight banks, bank 0 is the lower 32K bytes dynamic RAM, bank 1 is the VRAM bank and bank 7 is the ROM bank which is the BOOT ROM.

The two 74HC157, IC24 and IC25, are there to provide multiplexing function to address the high and low order 16 bits system address bus through the control signal MPX.

The Din and Dout of each of the 4164 RAM is connected together to facilities efficient circuit design. Therefore early write method is used in BW2 to allow the R/W of data. The \overline{RD} signal from the CPU is connected to the \overline{WE} pin of the RAM chip via an inverter, the direction of data flow is determined by the line.

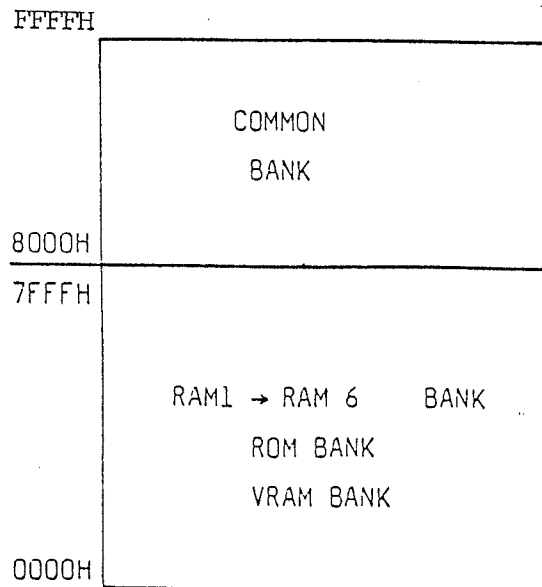


Fig 2.4 Memory Map of Bondwell 2

2.2.6 VRAM & LCD DISPLAY

The VRAM used in the BW2 are the static RAM HM6116 (IC50 to IC57), they can be directly accessed by the CPU when DIEN of the LCD controller (pin 39, MSM6255, IC49) is low. The 16K VRAM is addressed by MA0 to MA13 from 6255 where MA0 to MA10 are directly connected to the memory chips and MA11 to MA13 are connected to the address decoder (HC138, IC48) which enables the memory chips one at a time.

In the later version, two HM6264P are used instead of the eight 6116P.

The data access between the VRAM and the CPU is done through a tri-state transceiver (HC245, IC47). The transceiver is enabled by a low on \overline{G} (pin 19, IC47) which is signified by a low on VRAM. Data transfer is then possible after the chip is activated. Direction of the data flow is controlled by the logic level of DIR. When DIR is low, data flow from B input (CPU) to A output (VRAM), when DIR is high, data flow from A input (VRAM) to B output (CPU).

The ADF of the LCD controller (pin 40) is pulled high to allow address A0 - A13 output to MA0 - MA13 while \overline{DIV} is set low for external clock application (16MHz to pin 65).

Data is input to the LCD controller through the input RD0 to RD7 directly from VRAM bus which is then fed to the LCD module via the display data parallel output (pin 33 - 36).

The LCD module is connected to the LCD controller (IC49) with a 12 way flat cable. The LCD module is a high resolution 640 x 200 dots matrix display.

The driving method of the LCD is ODD - EVEN mode which consists of 4 data lines from the 6255 (UD0 - UD3). Where UD0 and UD2 control the even dot bits of the LCD display while UD1 and UD3 control the odd dot bits. UD1 and UD2 take care of the upper half of the screen. UD3 and UD4 take care of the lower half of the screen. The Frame, DF, Load, CP are the signals for screen control and refreshing.

For detail of the LCD controller, please refer to Chapter 4 Section 4.4.

2.2.7 PARALLEL I/O

The parallel I/O in Bondwell 2 is a 82C55 which functions to select memory bank, scan keyboard, select drive and control several other I/O signals.

PC0 to PC2 are decoded by a HC138 to select one of the 8 memory banks. In these 8 banks, RAM1 is the system RAM bank which has address from 0H to 7FFFH. VRAM is the 16K bytes LCD refresh memory. RAM2 to RAM6 are connected to the gold-finger slot for expansion. The ROM bank selects the boot-ROM. PC0 to PC2 are pulled high so that when power up, ROM bank is selected.

PC3 is the only port that have no connection. PC4 receives the BUSY signal from external printer and PC5 receives a motor feed back signal generated by the motor on signal. PC6 senses the data carrier detect signal from RS232 port. PC7 detects the write protect signal generated from the floppy disks.

PA0 to PA3 is decoded by a decimal decoder 7445 (IC42) to drive the row address of the keyboard. PB0 to PB7 read the scanned keyboard to see if any key being pressed. The matrix of the keyboard is in the Appendix A.

PA4 and PA5 is the drive select signal to the floppy drives. PA6 selects between RS232 port at the back of the computer and that at the gold-finger. PA7 sends a stroke signal to the printer port, which indicates the validity of data to the printer.

2.2.8 FLOPPY DISK CONTROLLER

The 2797 (IC5) floppy disk controller (FDC) is an NMOS device, its current consumption is typically 70mA. In fact the FDC is used only when the floppy disk drive is being accessed. Therefore a power saving feature is incorporated so that if the floppy is idle for more than 10 minutes, the power supply to the FDC is cut. When accessing the floppy disk is needed, the motor-on MTRON (DWG A6) signal is first issued. The power board recognises the motor-on signal as an indication of accessing floppy, it then turns on the power of the FDC. Upon power up, the self-reset circuit of the FDC issues a reset delay to itself. This will cause the FDC to reinitialize itself.

The data transfer rate of micro floppy disk drive to 250K bits/sec and the clock generator by 2797 is 1 MHz. Distinguished from other FDCs, 2797 contains an internal data separator and write precompensation circuit. The Test (pin 22) line is used to adjust both data separator and precompensation. When Test = 0, the WD (pin 31) line is internally connected to the output of the write precomp one-shot. Adjustment of the WPW (pin 33) line can then be accomplished. A second one-shot tracks the precomp setting at approximately 3:1 to insure adequate write data pulse widths to meet drive specifications.

Data separation is also adjusted with Test = 0. The TG43 (pin 29) line is internally connected to the output of the read data one-shot, which is adjusted via the RPW (pin 18) line. The DIRC (pin 16) line contains the read clock output (250KHz). The VC0 trimming capacitor (pin 26) is adjusted for centre frequency. For detail description of 2797 calibration, please refer to testing procedures of BW2 in Chapter 3.

In the Bondwell 2, the CPU clock frequency is 2 MHz. When writing or reading data to or from the floppy disk drive, the worse case that the CPU has to serve the FDC is 27 usec when reading, and 23 usec when writing. These figures are not sufficient for the 2 MHz CPU to perform transferring one byte of data and increment and decrement various counters. So the method of interrupt I/O is used instead of programmed I/O.

Pin 38 DRQ is a data request signal. When the FDC wants a byte transfer, this signal is used to interrupt the CPU. Pin 39 INTRQ is interrupt request signal which goes high when a command execution in the FDC is finished. Ordinarily, CPU interrupt is disabled at the time of power up and is only enabled in the format disk program to indicate the termination of formatting one track.

2.2.9 SYSTEM CLOCK GENERATOR

The Bondwell 2 incorporates an 16 MHz crystal to produce the necessary clock frequency for the various system devices. The inverter HCU04 is used together with the crystal to produce the 16 MHz clock signal which is fed to the LCD controller and to a 4-bit binary counter which divide the signal into 8MHz, 4MHz, 2MHz and 1MHz. 4MHz is used by the Programmable Interval Timer 82C53. The 2MHz clock is used by the USART and the CPU (Ver. 1.0) while the 1MHz is the clock signal supplied to the Floppy Disk Controller.

2.2.10 PROGRAMMABLE INTERVAL TIMER (PIT)

The programmable timer of the Bondwell 2 is a 82C53 which has three 16 bit counters inside.

Counter 0 is used as the transmit $\overline{\text{TXC}}$ and receive $\overline{\text{RXC}}$ clock of 82C51 USART. OUT 0 is a square wave output dividing the 4MHz CLK 0 input by the counter value. It determines the transfer speed of the transmit/receive data.

CLK 1 is derived from the LCD controller (pin 24, IC49, DWG A4) and has clock signal value of 11 KHz feeding to counter 1. After divided by the counter value, it is a 3Hz square wave signal at OUT 1. This 3Hz output is directed to the power on LED indicator through IC38. When the battery goes low, the comparator on the power board send out a low voltage signal $\overline{\text{LVOP}}$. As a result the LED blinks to show battery-low status.

The output of counter 1 is also the input of counter 2, CLK 2. Counter 2 is a monostable output working as a motor on $\overline{\text{MTRON}}$ signal which gives a second delay for the motor to turn off after $\overline{\text{MTRON}}$ goes high, Fig 2.5 Counter 2 is also the signal for turning on the power of the $\overline{\text{FDC}}$ after it has been shut down.

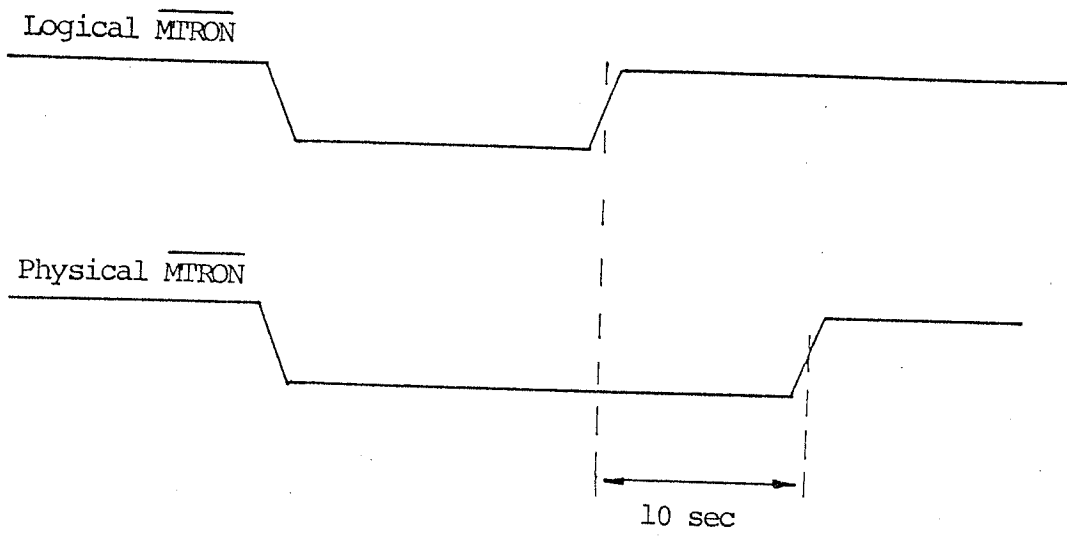


Fig. 2.5 $\overline{\text{MTRON}}$ Delay

2.2.11 PRINTER AND SERIAL I/O

The printer interface is performed by a HC273 (IC27) and two buffer ICs (IC37, 38). When data is latched to the HC273, the 8255 (IC4) sends a STB pulse to the printer indicating the validity of data at the printer port. The BUSY signal tells the 8255 the status of the printer.

The serial I/O in Bondwell 2 is performed by a 82C51 USART. The USART receives parallel data from the CPU and transmits serial data after conversion. The device also receives serial data from external devices and transmits parallel data to the CPU after conversion. The data lines of the USART are all level shifted by the line driver 1488 and line receiver 1489 (IC43 and IC44) to meet the standard RS232C specifications.

The SELECT signal from the 8255 choose between the input and the output mode of the RS232C port. When the SELECT is high, the B inputs of the IC45 is connected to the Y outputs (which is turn enable receiving function of the RS232C port). When SELECT goes low, gates A are connected to Y output gates (and RS232C port enters into transmitting mode).

2.2.12 POWER BOARD

The power in the Bondwell 2 is supplied by a built-in rechargeable battery of 12V 2.6AH. External power adaptor can be connected to the battery to recharge it through the D.C. jack at the back of the computer. Two switching circuit convert the 12V to 5V and -13V.

3.4AH

A voltage detector ICL8211 (IC1) detects the voltage level of the battery. If the battery drops below 10.5V (or any preset value), the LVOP (pin 4) goes to a low level, which together with the 3Hz pulse from the PIT 8253 makes the power-on LED blink to indicate battery low state. Detail of how to calibrate the low volt reference value is shown in Chapter 3.

The 5V output of the system is supplied through a L296 (IC2). The L296 is a monolithic switching regulator. The L296 regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference Zener Zap trimmed to $\pm 2\%$. This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. Precision and frequency stability of the loop is adjustable by an external RC network connected to pin 9.

The -13V output of the Bondwell 2 is supplied by a TL497AC (IC3) which is a fixed-on-time variable-frequency switching voltage regulator control circuit. The on time is programmed by an external capacitor connected between the frequency control pin (pin 3) and ground. The output voltage is controlled by an external resistor ladder network (R9, R10 and VR2). The -13V is solely for the supply to the LCD module and on-board 1488 chip.

The +12V supply is regulated through the high current linear regulator 7812 (IC5) which is, at the same time, the pre-regulator for the input of TL497AC. Though in the earlier version, it may be noticed that the +12V supply is taken directly from the battery and the pre-regulator for IC3 is 78L12.

The BW2 energy saving circuitry is constructed by using timer TLC555 (IC4) and it's associated components.

When the EN5V* goes low, the O/P (pin 3) of IC4 goes high which turns on the transistor T2 closing the relay RRD51A05. The +5V* is so connected to the +5V rail. The +5V* is the power supply to the FDC and the FDC driver/receiver.

When the EN5V* goes high turning off the transistor T1. The capacitor C18 is then charged up through R16. The capacitor is initially discharged when T1 is turned off when EN5V* is low. When the voltage of C18 is greater than two-third of 5V, the output of the TLC555 will go low which turns off the transistor T2 as well as the relay. The path from the +5V to the +5V* is opened cutting off the power supply to the FDC and FDC driver/receiver. The time delay to turn off +5V* is determined by the value of R16 and C18 and is typically 5 minutes.

CHAPTER 3 SYSTEM TROUBLESHOOTING

3.1 INTRODUCTION

This chapter provides all information necessary to troubleshoot the Bondwell 2 Lap Size Computer on the subsystem level. However, the following initial checks must be performed before the troubleshooting begins.

- 1) Use software which is known to be good in order to determine if the problem is hardware or software related.
- 2) Perform a visual check prior to digging into the circuitry. That is, check for blown fuse, broken or burned components, damaged connectors, intermittent switches, etc. and other obvious defects.

3.1.1 INITIAL CHECKS

A self-test routine resided in the BIOS ROM is automatically performed each time the power is turned ON.

After ensuring the Bondwell 2 is properly set-up, switch on power (Power Switch is located on the left hand side of machine) for the system unit. The self-test routine begins to run.

Normally the monitor should display :

"64K RAM is installed"
and the system will urge you to put in a system diskette to load system.

If all system components are in full functional order. The display will show "pass all testes loading system".

The self-test routine resides within the BIOS ROM covers the areas of System RAM, VRAM, PIO, TIMER, USART, LCD controller and FDC.

If the system encounters any fault in the testing procedure, whether it is caused by defected components or any other reasons. The system will fail the self-test routine and display an error message of the related area will be displayed on the screen.

The message shown on screen might be one (or more) of the followings :-

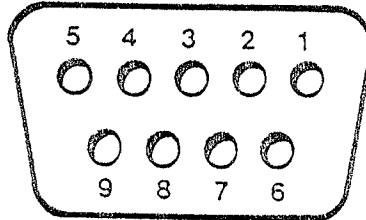
1. System RAM test fail
2. VRAM test fail
3. LCD controller test fail
4. PPI test fail
5. Counter test fail
6. USART test fail
7. FDC test fail
8. DRIVE A fail

The above messages indicates that the system fails to communicate with the particular device when they are called upon. They are aimed to provide a general direction where the trouble lies.

However, before starting any troubleshooting procedure, one must make sure whether the fault is a hard failure or not. This can be done simply by turning the power off and switch-on the power again. If the symptom persists, then start trouble-shoot the main board or the concerned area by following the troubleshooting flow-chart in the next section.

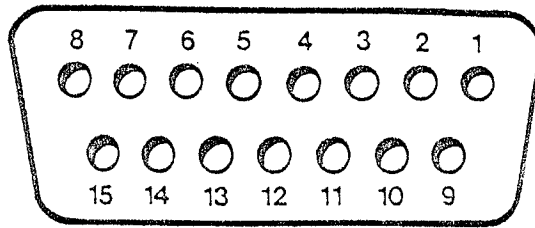
3.2 EXTERNAL DEVICE CONNECTOR WIRING DIAGRAM

3.2.1 RS-232C SOCKET PIN ASSIGNMENT (FRONT VIEW)



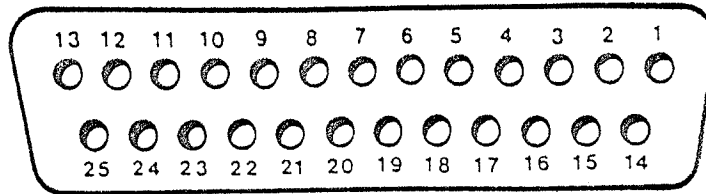
PIN NUMBER	SERIAL
1	GND
2	TRANSMIT DATA
3	RECEIVE DATA
4	REQUEST TO SEND
5	CLEAR TO SEND
6	DATA SET READY
7	GND
8	DATA CARRIER DEFECT
9	DATA TERMINAL READY

3.2.2 CENTRONICS-TYPE PRINTER PORT PIN ASSIGNMENT
(FRONT VIEW)



PIN NUMBER	SIGNAL
1	STROBE
2	DATA 0
3	DATA 1
4	DATA 2
5	DATA 3
6	DATA 4
7	DATA 5
8	DATA 6
9	DATA 7
10	GND
11	BUSY
12	GND
13	GND
14	GND
15	GND

3.2.3 DISK DRIVE EXPANSION PORT PIN ASSIGNMENT
(FRONT VIEW)

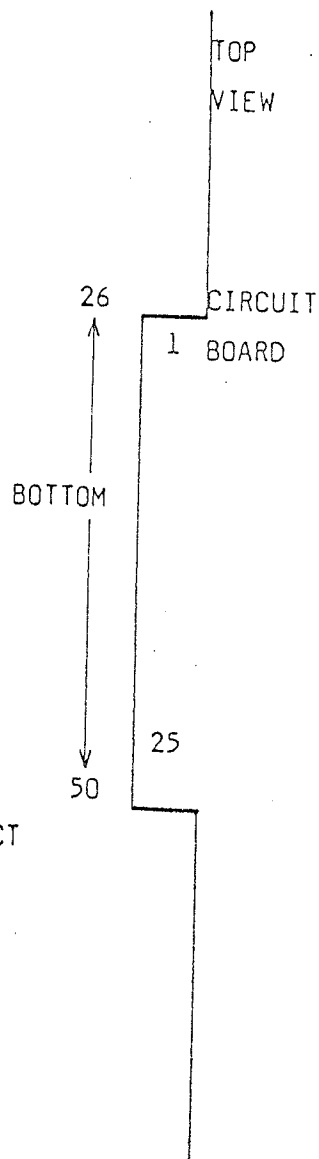


PIN NUMBER	SIGNAL
1	+12V
2	+5V
3	+5V
4	$\overline{\text{INDEX}}$
5	$\overline{\text{DRIVE SELECT 1}}$
6	$\overline{\text{DIRECTION}}$
7	$\overline{\text{STEP}}$
8	$\overline{\text{WRITE DATA}}$
9	$\overline{\text{WRITE GATE}}$
10	$\overline{\text{TRACK } \emptyset\emptyset}$
11	$\overline{\text{WRITE PROTECT}}$
12	$\overline{\text{READ DATA}}$
13	SIDE SELECT

14	+12V
15	+12V
16	+5V
17	$\overline{\text{DRIVE SELECT } \phi}$
18	$\overline{\text{MOTOR ON}}$
19	$\overline{\text{READY}}$
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND

3.2.4 EXPANSION SLOT PIN ASSIGNMENT

J18 EDGE CON.			J19 EDGE CON.		
5V	1	26	12V		
D3	2	27	12V		
A1	3	28	A3		
A2	4	29	A4		
<u>CTS8</u>	5	30	A5		
<u>RST</u>	6	31	A6		
<u>MODESEL</u>	7	32	A7		
<u>16MHZ</u>	8	33	A8		
<u>IORQ</u>	9	34	A9		
<u>RD</u>	10	35	A10		
D0	11	36	A11		
D1	12	37	A12		
D2	13	38	A13		
A0	14	39	A14		
D4	15	40	<u>RAM6</u>		
D5	16	41	<u>RAM5</u>		
D6	17	42	<u>RFSH</u>		
D7	18	43	<u>WR</u>		
DCDB	19	44	SELECT		
<u>DTRB</u>	20	45	<u>RAM2</u>		
<u>RTSB</u>	21	46	<u>RAM3</u>		
<u>DSRB</u>	22	47	<u>RAM4</u>		
TXDB	23	48	<u>SLOT</u>		
RXDB	24	49	GND		
GND	25	50	5V		



3.3 FAULT ISOLATING FLOW CHART

Whenever experiencing any kind of malfunction on the BW2. The following fault-isolating flow chart and the Remarks in the following page enable a quick and systematic approach to locate and correct the fault.

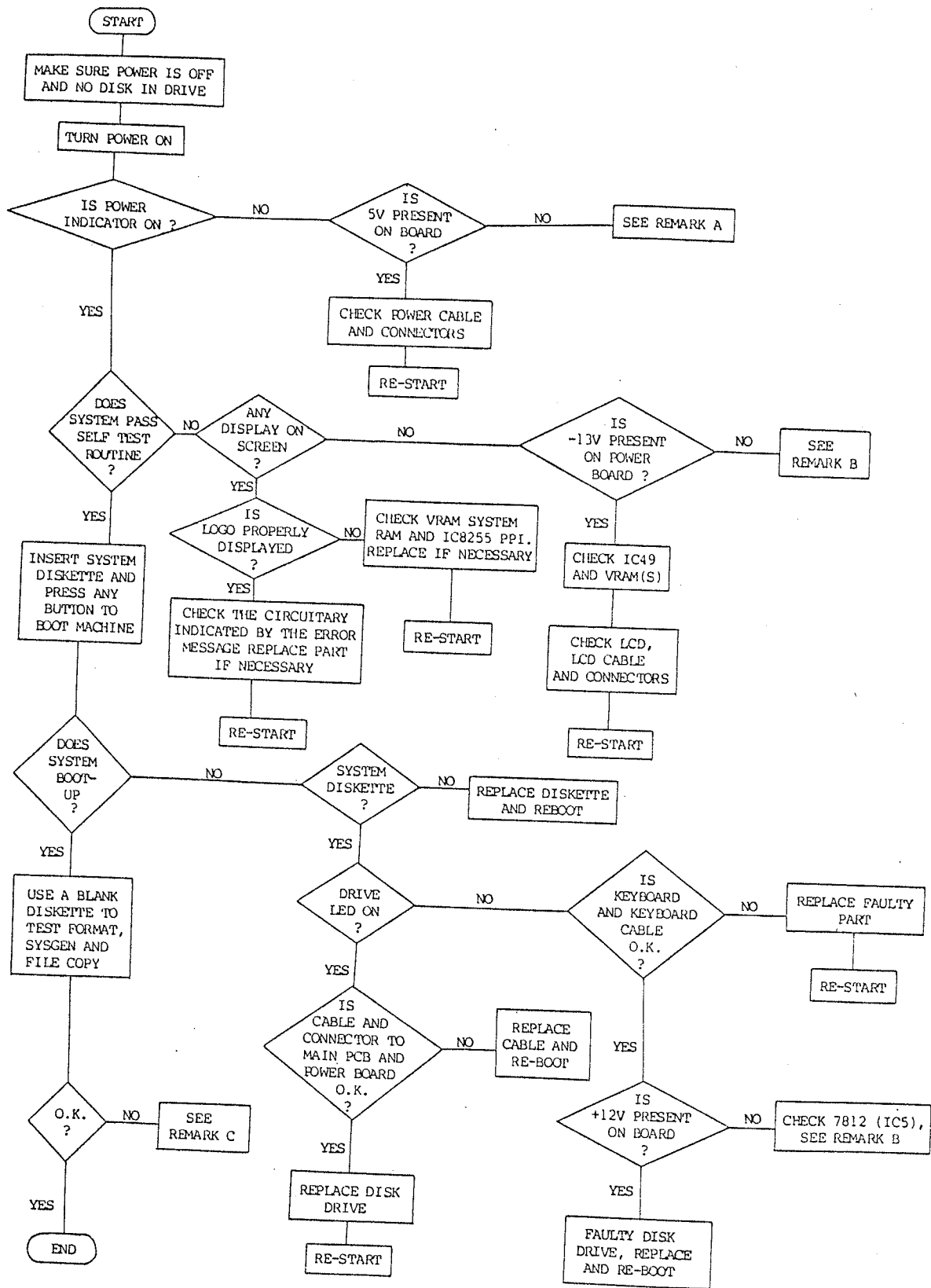


Fig. 3.1 Fault Isolating Flow Chart

REMARKS :

- A. i) Check switching regulator pin 11 of IC2 L296 for oscillation. The output should be a saw tooth waveform of 60KHz.
- ii) Check pin 2 of the above IC, the output should be a 60KHz square waveform.
- B. i) Check the output of IC5 7812 (PCB version 1.5) for +12V.
- ii) Check pin 3 of IC3 TL497AC switching regulator for a periodic output in the following form.
- iii) Check also the output of pin 7 for square wave.
- C. i) Check the timing frequency and pulse width of the variable capacitor J14 and the two variable resistors J15 and J16 is of the correct specification and calibrate accordingly.
- Adjust J15 (10KVR) so that the pulse width on FDC pin 31 is 250ns + 10ns.
- Adjust J16 (50KVR) so that the pulse width on FDC pin 29 is 500ns + 20ns.
- Adjust J14 (VC) to set the frequency of pin 16 FDC to 250KHz + 1KHz.
- ii) Check the +5V * to FDC and verify the signal source from the power board and the Programmable Interval Timer 82C53 IC6.

3.4 GENERAL TROUBLESHOOTING TECHNIQUE

1. When going to the suspected area of the main PCB, you should perform output to input check until the bad signal is located.
2. If the symptom indicated is not very obvious or is difficult in deciding where to start troubleshooting, then you should start with the clock generator and CPU as shown in Schematic DWG A1 and check for signal activity.
3. You could swap parts or even a sub-assembly to simplify a complicated problem.

3.5 DISASSEMBLY/ASSEMBLY PROCEDURE

1. Unscrew the four screws at the bottom of machine and the two at the inside of the carrying handle mounting plate.
2. Separate the machine top and bottom cabinets by pressing inward to unlock the hooks which are located on the bottom cabinet rim.

HINT : it is easier to undo the hook on the left hand side (direction key side) of the machine first. Fig. 3.2 shows the location of the screws and hooks.

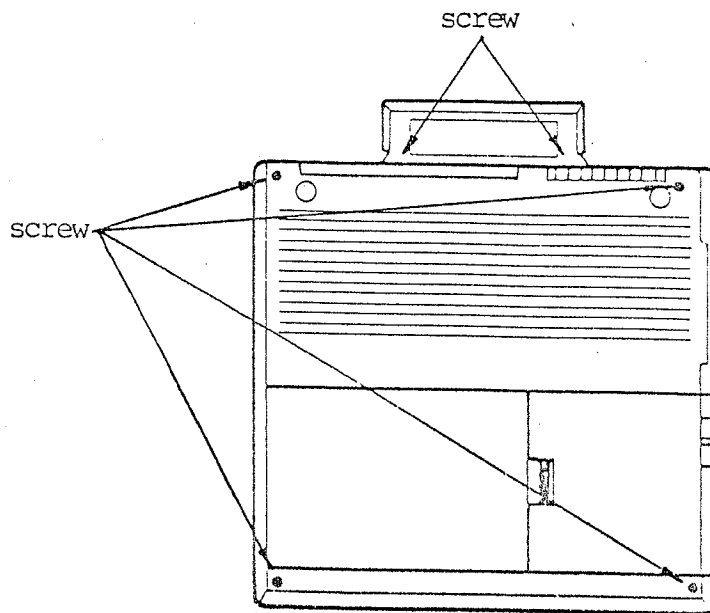
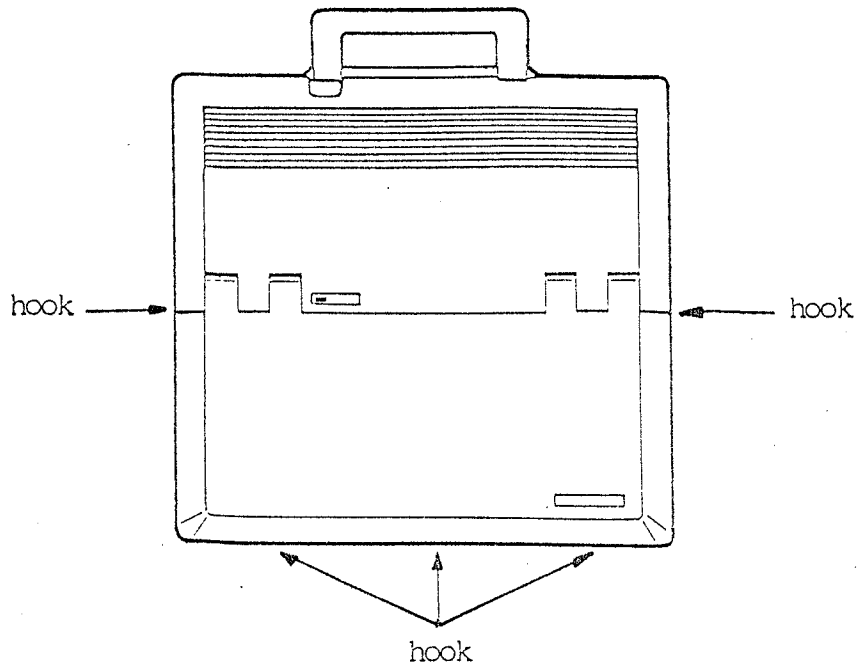


Fig. 3.2 Screws and Hooks Location of Bondwell 2

3. Rest the machine on its base and gently lift up the top cabinet.
4. Disconnect the keyboard cable from the keyboard assembly P.C.B.
5. Disconnect the LCD module connecting cable from the main P.C.B. mounted on the base of main unit.
6. Undo the screw that hold the 'Power On' LED indicator and release it from its housing.

Top cabinet can be completely free from the base unit.
7. To separate the keyboard unit, release the four screws on the keyboard template (metal plate) that hold the unit to the top cabinet. Keyboard can then be free from top cabinet housing.
8. On the inside of the top cabinet there are two screws (with compression spring) that hold the LCD module to the machine. Undo these screws to release the module from cabinet.
9. Rest the LCD module unit on a flat surface with LCD facing upward. Undo the six screws and the four hex screws mounted on the front plate. Put away the LCD front cabinet and direct access to the LCD module is possible.

Bottom Unit :-

10. unscrew the four screws that hold the microfloppy disk drive and disconnect all the sockets to the disk drive. Free the drive unit from bottom cabinet.

11. Release the rechargeable battery by undoing the two screws that holds the battery by the metal fastening plate. At the same time, gently lift off the power supply board (the small p.c.b. situated vertically adjacent to the battery) together with the power supply socket.

12. Undo all the screws on the main board and handle mounting plate that hold the main p.c.b. to the base of bottom cabinet. Gently lift up the p.c.b. and disassembly procedure is completed.

13. Re-assembly procedure is reverse to disassembly procedure.

3.6 BONDWELL 2 HARDWARE SPECIFICATION

3.6.1 MAIN BOARD

The diagnostic on the BOOT ROM, as mentioned in the earlier section, must be passed, which include :

System RAM test,
Video RAM test,
PPI test,
USART test,
TIMER test,
FDC test,
LCD CONTROLLER test, and
Disk Drive A test.

3.6.2 POWER CONSUMPTION

The power consumption of main board with keyboard, LCD module and floppy disk drive disconnected.

+5V - less than 400 mA
+12V - less than 30 mA
-12V - less than 31 mA

3.6.3 CLOCK FREQUENCY

16 MHz (IC33 pin 6)	-	± 0.1%
4 MHz (IC33 pin 13)	-	± 0.1%
2 MHz (IC33 pin 12)	-	± 0.1%
1 MHz (IC33 pin 11)	-	± 0.1%

Output level : high > 4.5V
low < 0.2V

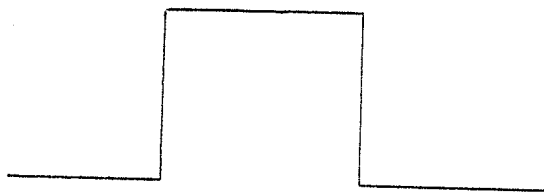
3.6.4 WRITE PULSE WIDTH, READ PULSE WIDTH AND DATA RATE

When $\overline{\text{TEST}}$ pin (FDC 2797 pin 22) strobe low :

Note : Steady state - 30 seconds after power on.

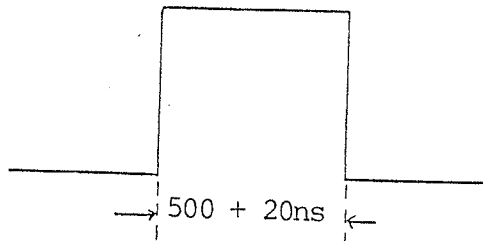
pin 16 of FDC - $250\text{KHz} \pm 1\text{KHz}$ (at steady state)

pin 16 of FDC - $250\text{KHz} \pm 10\text{KHz}$ (at any other time)

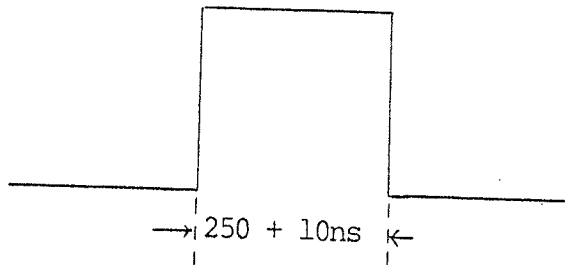


$250 \pm 1\text{KHz}$ at steady state

Pin 29 of FDC - $500\text{ns} \pm 20\text{ns}$



Pin 31 of FDC - $250\text{ns} \pm 10\text{ns}$



3.6.5 FDC (2797 IC5) TESTING AND ADJUSTMENT PROCEDURE

- Jumper, J30 should be set to VCC at power up.
- After power on, switch J30 to the other position so that FDC pin 22 (TEST) is connected to GND.
- Observe FDC pin 31 with a CRO.
- The CRO is set to 50ns/div and 0.5V/div.
- Adjust J15 (10KVR) so that the pulse width on FDC pin 31 is 250ns \pm 10ns.
- Set the CRO to 100ns/div and 0.5V/div
- Observe FDC pin 29.
- Adjust J16 (50 KVR) so that the pulse width on FDC pin 29 is 500ns \pm 20ns.
- Use a frequency counter to measure the frequency on FDC pin 16.
- Adjust J14 (variable cap) to set the frequency to 250KHz \pm 1KHz.
- Switch the jumper back to the original position.
- Power off.

3.6.6 BONDWELL 2 SWITCHING POWER SUPPLY TESTING AND CALIBRATING PROCEDURES :-

i. Calibration spec. of switching power supply module

* The following tests are under the conditions of having DUMMY LOAD and HEAT SINK.

- supply voltage : 9.5V min. to 16V max.
+12.00V nominal
- line regulation (5V\$2A) : 20mV (typ.)
- load regulation (5V\$4A) : 15mV (typ.)
- output rise time : 100ms (typ.)
- RESET delay time : 100ms (typ.)
- current spec. : +5V \$2A
(max. operating) +12V \$700mA
-13V \$-45mA
- output current limit : +5V --> 4A (protected)
-13V --> -230mA (protected)
- (1) pin (11) of L296 : 60KHz \pm 10KHz Sawtooth
pin (2) of L296 : 60KHz \pm 10KHz square wave
(2) pin (3) of TL497AC : ramp waveform
pin (7) of TL497AC : square waveform
<Detail waveforms are shown in page 2>
- nominal output voltage : #1 +12V \$700mA
#2 +5V \$2A
#3 -13V \$-45mA
- output voltage variation : +5V (4.9V to 5.2V) o/c
+5V (4.75V to 5.25V) \$2A
+12V (9.5 to 16V) \$700mA
-13V (-12.00V to -13.50V)
\$-45mA
- output ripple : +5V \$2A 150mV p-p
-13V \$-45mA 150mV p-p
- heat sink temperature : under 90 °C (operating)

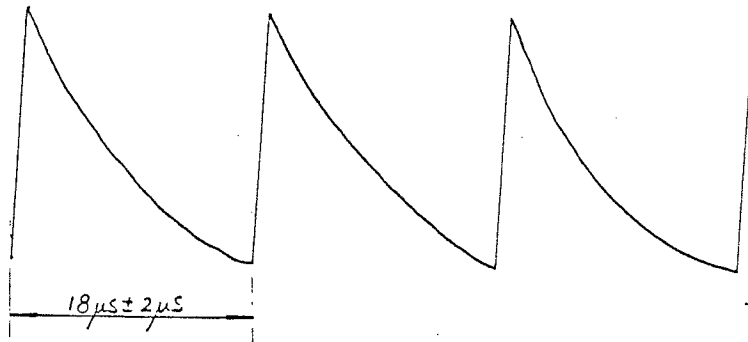
- PCB dimensions : 11.7cm x 6.9cm
- Final test for LVOP SHOULD obtain the following results :

LED flashing voltage : 9.6V to 10.2V
 LED lit voltage : 11V to 11.6V

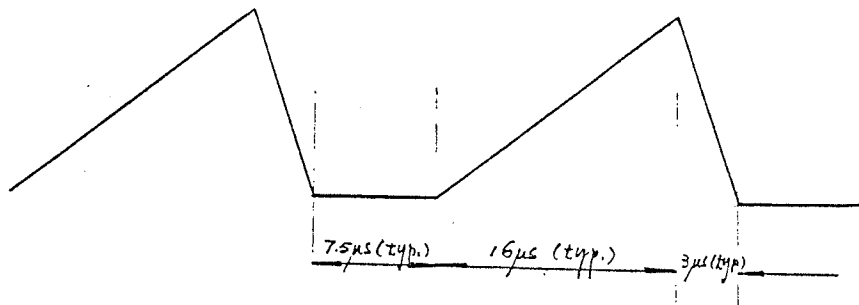
(When switching on the whole unit HANDBOOK, the LED must lit at all trials.)

Detail waveforms :

a) At pin(11) of L296,



b) At pin(3) of TL497AC,



ii. Calibrating Procedures :

- a) #3 -13V output voltage calibration :
 - 1) Set supply voltage of power board to $15V \pm 0.5V$.
 - 2) With the output at full load (-45mA), trim the output voltage to $-13V \pm 0.1V$.
 - 3) Vary the supply voltage to $9.5V + 0.2V$, output voltage SHOULD NOT be less than $-12.00V$.

- b) Low voltage calibration :
 - 1) Set supply voltage of power board to $9.80V$ sharp with a DVM.
 - 2) Probe pin (4) of IC1(ICL8211), LVOP, and use a plastic screw driver to trim VR1 in one direction to obtain a 'logic 1' ($4.5V$ min).
 - 3) With LVOP STILL at 'logic 1', trim VR1 in reverse direction very slowly until pin (4) of IC1 JUST switch to 'logic 0'.
 - 4) Fix the value of VR1 for subsequent testes.

* Final test for LVOP SHOULD obtain the following results :

LED flashing voltage (V_L) : $9.6V$ to $1.2V$
LED lit voltage (V_H) : $11.0V$ to $11.6V$

iii. Testing procedure for low volt output, LVOP :

- a) Set supply voltage to $+13V \pm 0.5V$ with a DVM.
- b) Probe pin (4) of IC1(ICL8211) to note a 'logic 1'.
- c) Gradually decrease supply voltage to power board until pin (4) JUST switches to 'logic 0'.
- d) Check the value of the supply voltage, V_L
It must be : $9.6V < V < 10.2V$
- e) In the same way, increase the supply voltage gradually until pin (4) JUST switches back to 'logic 1'.
- f) Check the value of the supply voltage, V_H
It should be : $11.0V < V < 11.6V$

3.6.7 DISK DRIVE

1. Power Consumption

+12V	: Standby	1mA (max.)	
	Average at read/write		: 85mA (typ.) 180mA (max.)
	Average at seek		: 200mA (typ.) 260mA (max.)
	Peak at spindle motor start		: 300mA (max.)
+5V	: Average at read /write		: 140mA (typ.) 170mA (max.)
	Average at seek		: 100mA (typ.) 120mA (max.)

2. Motor speed : 300 r.p.m. \pm 1%

3. Alignment specification (using a commercially available alignment disk).

Radial alignment lobe rate : 80% min
Index to data burst : 200 usec + 100 usec
Hysteresis : 20% max
Head azimuth angle : \pm 18°
Asymmetry (track 0, track 39) : 600 nsec

CHAPTER 4 PROGRAMMABLE DEVICES

This chapter describes some of the programmable devices in the Bondwell 2 from the programming point of view. All the necessary information are included. However, the reader should be familiar with the Bondwell 2 and the Z-80 assembly language programming.

4.1

8253, THE PROGRAMMABLE INTERVAL TIMER

To the programmer, the 8253 counter/timer appears as four memory locations or I/O ports. These are selected as follows :

\overline{CS}	A0	A1	Function
0	0	0	Select counter/timer 0
0	0	1	Select counter/timer 1
0	1	0	Select counter/timer 2
0	1	1	Select Control Register

Since the Read Control signal RD is tied permanently to +5V by hardware, the 8253 is limited to the following manipulation :

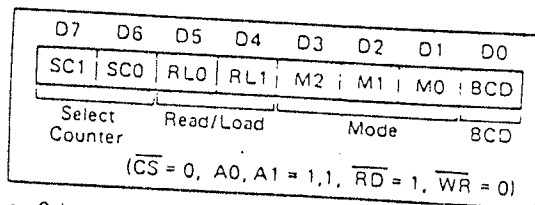
\overline{CS}	\overline{RD}	\overline{WR}	A1	A0	Function
0	1	0	0	0	Load counter/timer 0
0	1	0	0	1	Load counter/timer 1
0	1	0	1	0	Load counter/timer 2
0	1	0	1	1	Write Mode Word
0	1	1	X	X	No Operation, 3-state

The modes for each counter are programmed by selecting each timer-register address and writing the correct control word for format is shown in the following chart.

4.1.1 8253 PROGRAMMABLE INTERVAL TIMER CONTROL WORD

Control Word and Count Value Program

Each counter operating mode is set by control word programming. The control word format is outlined below.



- Select Counter (SC0, SC1): Selection of set counter

SC1	SC0	Set Contents
0	0	Counter = 0 selection
0	1	Counter = 1 selection
1	0	Counter = 2 selection
1	1	Illegal combination

- Read/Load (RL1, RL0): Count value Reading/Loading format setting

RL1	RL0	Set Contents
0	0	Counter Latch operation
0	1	Reading/Loading of Least Significant byte (LSB)
1	0	Reading/Loading of Most Significant byte (MSB)
1	1	Reading/Loading of LSB followed by MSB

- BCD: Operation count mode setting

BCD	Set Contents
0	Binary Count (16-bits Binary)
1	BCD Count (4-decades Binary Coded Decimal)

- Mode (M2, M1, M0): Operation waveform mode setting

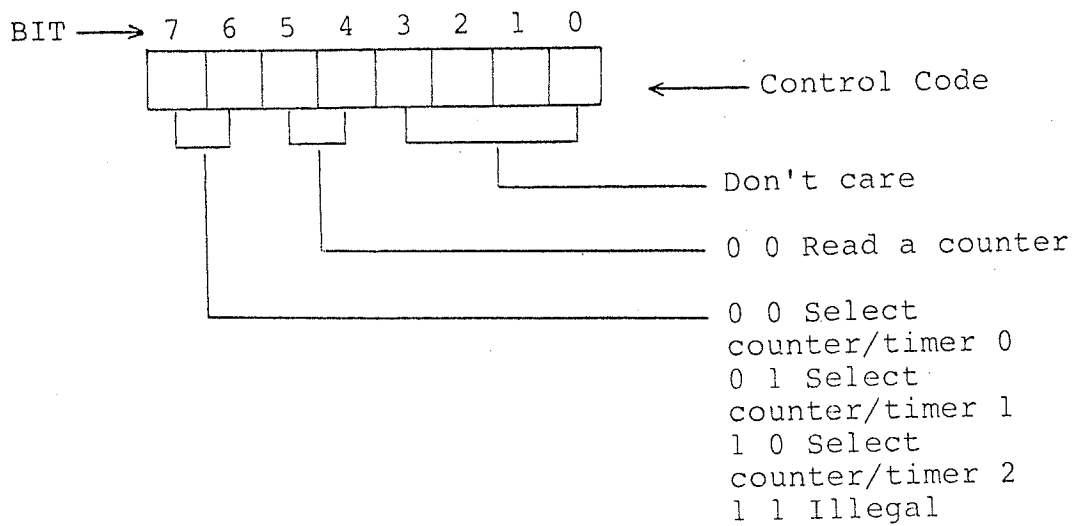
M2	M1	M0	Set Contents
0	0	0	Mode 0 (Interrupt on Terminal Count)
0	0	1	Mode 1 (Programmable One-Shot)
x	1	0	Mode 2 (Rate Generator)
x	1	1	Mode 3 (Square Wave Generator)
1	0	0	Mode 4 (Software Triggered Strobe)
1	0	1	Mode 5 (Hardware Triggered Strobe)

x denotes "not specified".

4.1.2 MONITORING 8253 COUNTER/TIMER OPERATION

The 8253 counter/timer has no Status register. Therefore, operation is monitored by reading the contents of any counter register, at any time. Below shows a reading technique.

If you want to read a counter's contents while it is decrementing, then you must write the following command code to the counter/timer.



Writing in the following instruction sequence, you will read the contents of counter on the fly.

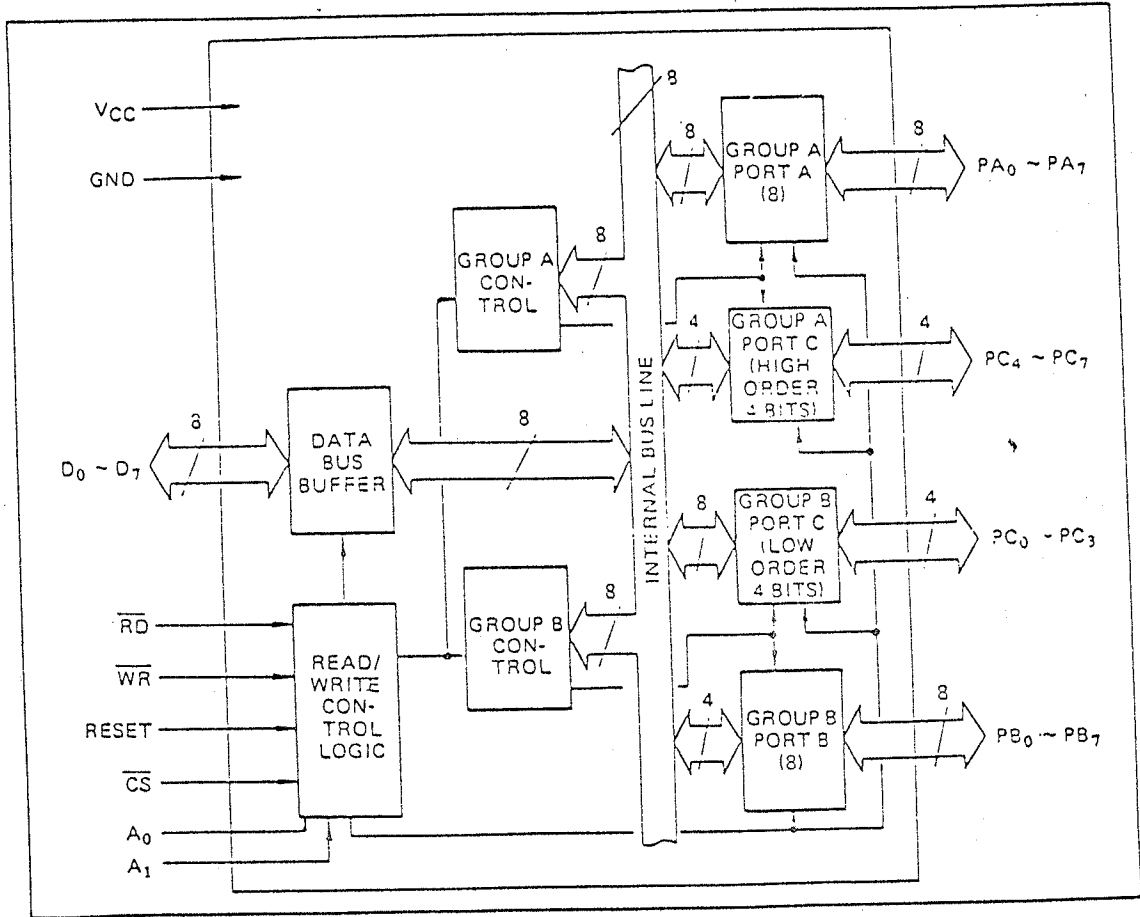
```
LD    A, 40H ; output control code to read
OUT   (7), A ; counter 1 contents
IN    A, (5) ; Read counter 1 contents and
LD    C, A   ; store in BC
IN    A, (5)
LD    B, A
```

4.2 82C55, CMOS PROGRAMMABLE PERIPHERAL INTERFACE

This device provides effective means to interface peripheral equipment such as the keyboard and a high speed printer to the Z80 CPU through the 24-bit I/O pins, which is equivalent to three 8-bit bidirectional buses, and the control lines.

The following diagram shows the circuit configuration.

CIRCUIT CONFIGURATION



BASIC FUNCTIONAL DESCRIPTION

Group A and Group B

When setting a mode to a port having 24 bits, set it by dividing it into two groups of 12 bits each.

Group A: Port A (8 bits) and high order 4 bits of port C (PC7 ~ PC4)

Group B: Port B (8 bits) and low order 4 bits of port C (PC3 ~ PC0)

Mode 0, 1, 2

There are 3 types of modes to be set by group as follows:

Mode 0: Basic input operation/output operation (Available for both groups A and B)

Mode 1: Strobe input operation/output operation (Available for both groups A and B)

Mode 2: Bidirectional bus operation (Available for group A only)

When used in mode 1 or mode 2, however, port C has bits to be defined as ports for control signal for operation ports (port A for group A and port B for group B) of their respective groups.

Port A, B, C

The internal structure of 3 ports is as follows:

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch

Port B: One 8-bit data input/output latch/buffer and one 3-bit data input buffer

Port C: One 8-bit data output latch/buffer and one 3-bit data input buffer (no latch for input)

Single bit set/reset function for port C

When port C is defined as output port, it is possible to set (to turn to high level) or reset (to turn to low level) any one of 8 bits individually without affecting other bits.

OPERATIONAL DESCRIPTION

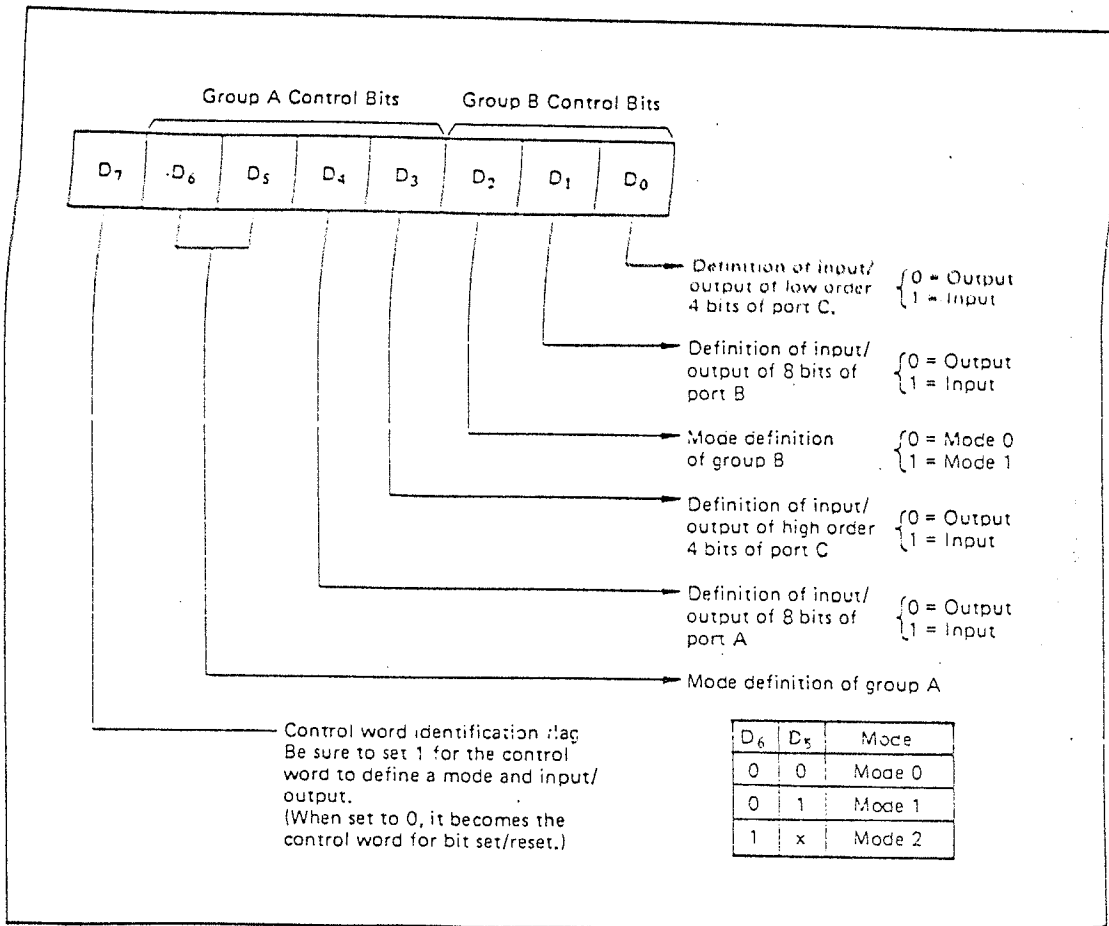
Control Logic

Operations by addresses and control signals, e.g., read and write, etc. are as shown in the table below:

Operation	A1	A0	\overline{CS}	\overline{WR}	\overline{RD}	Operation
Input	0	0	0	1	0	Port A → Data Bus
	0	1	0	1	0	Port B → Data Bus
	1	0	0	1	0	Port C → Data Bus
Output	0	0	0	0	1	Data Bus → Port A
	0	1	0	0	1	Data Bus → Port B
	1	0	0	0	1	Data Bus → Port C
Control	1	1	0	0	1	Data Bus → Control Register
Others	1	1	0	1	0	Illegal Condition
	x	x	1	x	x	Data bus is in the high impedance status.

Setting of Control Word

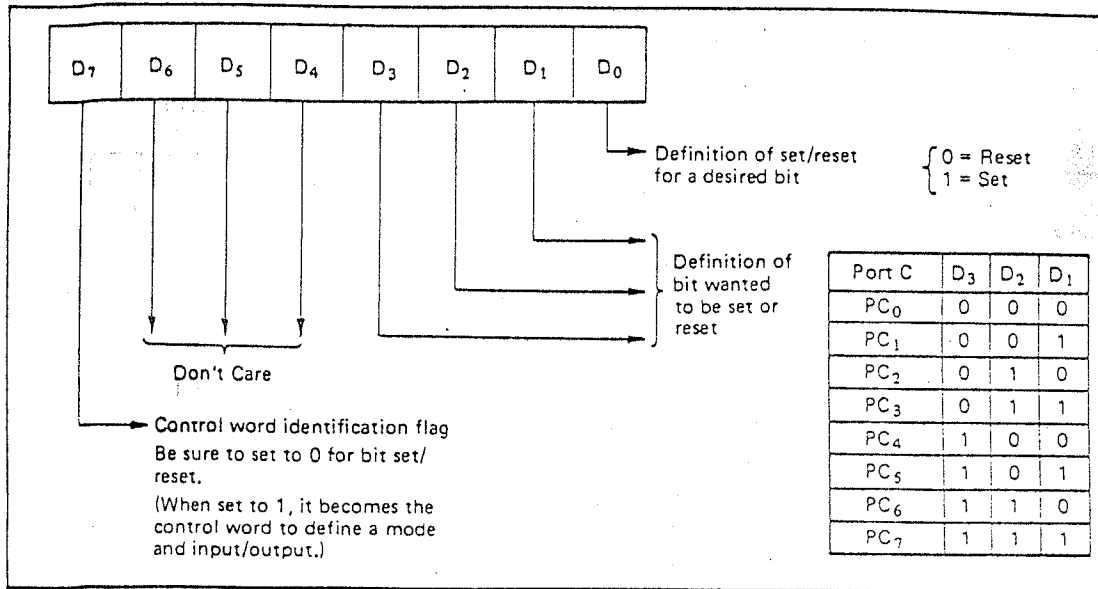
The control register is composed of 7-bit latch circuit and 1-bit flag as shown below.



Bit Set/Reset Function

When port C is defined as output port, it is possible to set (set output to 1) or reset (set output to 0) any

one of 8 bits without affecting other bits



Interrupt Control Function

When MSM82C55A-5 is used in mode 1 or mode 2, the interrupt signal for CPU is provided. The interrupt request signal is output from port C. When the internal flip-flop INTE is set beforehand at this time, the desired interrupt request signal is output. When it is reset beforehand, however, the interrupt request signal is not output. The set/reset of the internal flip-flop is made by the bit set/reset operation for port C virtually.

Bit set → INTE is set → Interrupt allowed

Bit reset → INTE is reset → Interrupt inhibited

Operational Description by Mode

1. Mode 0 (Basic input/output operation)

Mode 0 makes MSM82C55A-5 operate as a basic input port or output port. As no control signal such as interrupt request, etc. is required in this mode. All of 24 bits can be used as two 8-bit ports and two 4-bit ports. Sixteen combinations are then possible for inputs/outputs. The inputs are not latched, but the outputs are.

Type	Control Word								Group A		Group B	
	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	Port A	High Order 4 Bits of Port C	Port B	Low Order 4 Bits of Port C
1	1	0	0	0	0	0	0	0	Output	Output	Output	Output
2	1	0	0	0	0	0	0	1	Output	Output	Output	Output
3	1	0	0	0	0	0	1	0	Output	Output	Input	Output
4	1	0	0	0	0	0	1	1	Output	Output	Input	Input
5	1	0	0	0	1	0	0	0	Output	Input	Output	Output
6	1	0	0	0	1	0	0	1	Output	Input	Output	Input
7	1	0	0	0	1	0	1	0	Output	Input	Input	Output
8	1	0	0	0	1	0	1	1	Output	Input	Input	Input
9	1	0	0	1	0	0	0	0	Input	Output	Output	Output
10	1	0	0	1	0	0	0	1	Input	Output	Output	Input
11	1	0	0	1	0	0	1	0	Input	Output	Input	Output
12	1	0	0	1	0	0	1	1	Input	Output	Input	Input
13	1	0	0	1	1	0	0	0	Input	Input	Output	Output
14	1	0	0	1	1	0	0	1	Input	Input	Output	Input
15	1	0	0	1	1	0	1	0	Input	Input	Input	Output
16	1	0	0	1	1	0	1	1	Input	Input	Input	Input

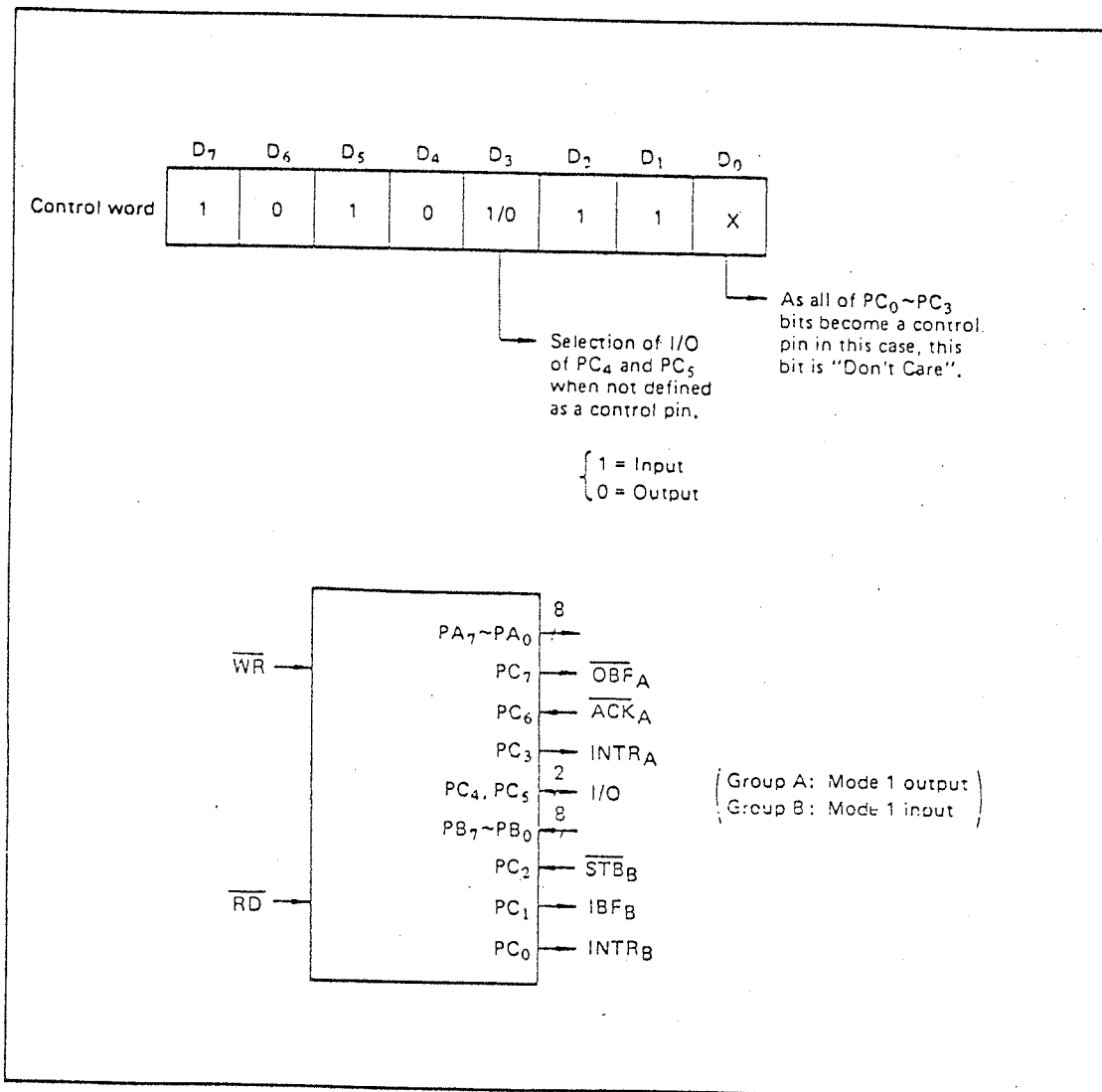
Note: When used in mode 0 for both groups A and B

Port C Function Allocation in Mode 1

Combination of Input/Output Port C	Group A: Input Group B: Input	Group A: Input Group B: Output	Group A: Output Group B: Input	Group A: Output Group B: Output
PC ₀	INTR _B	INTR _B	INTR _B	INTR _B
PC ₁	IBF _B	OBFB	IBF _B	OBFB
PC ₂	STB _B	ACK _B	STB _B	ACK _B
PC ₃	INTRA	INTRA	INTRA	INTRA
PC ₄	STBA	STBA	I/O	I/O
PC ₅	IBFA	IBFA	I/O	I/O
PC ₆	I/O	I/O	ACK _A	ACK _A
PC ₇	I/O	I/O	OBFA	OBFA

Note: I/O is a bit not used as the control signal, but it is available as a port of mode 0.

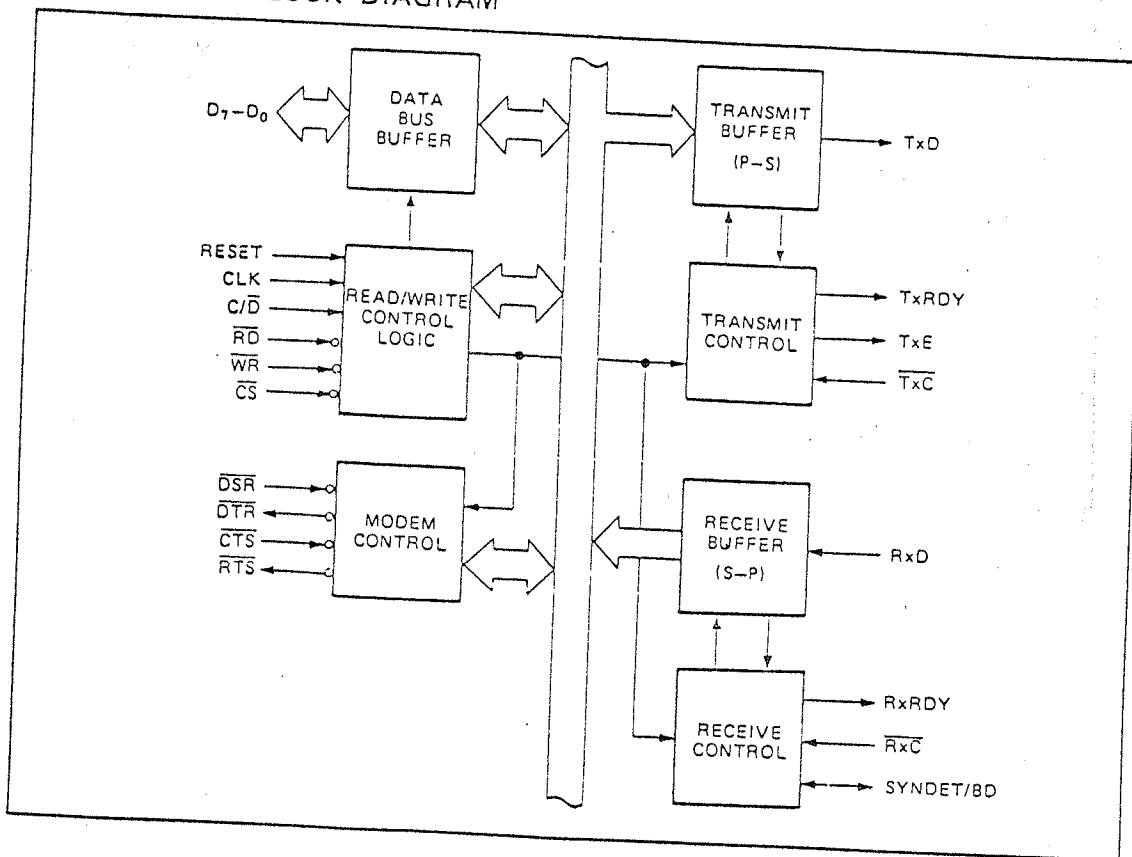
Examples of the relation between the control words and pins when used in mode 1 is shown below:
 (a) When group A is mode 1 output and group B is mode 1 input.



4.3 82C51 USART (UNIVERSAL SYNCHRONOUS ASYNCHRONOUS
RECEIVER TRANSMITTER)

The functional block diagram of the USART is shown in the following figures.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION

Outline

MSM82C51A's functional configuration is programmed by the software.

Operation between MSM82C51A and CPU is executed by program control. Table 1 shows the operation between CPU and the device.

Table 1 Operation between MSM82C51A and CPU

CS	C/D	RD	WR	
1	X	X	X	Data bus 3-state
0	X	1	1	Data bus 3-state
0	1	0	1	Status → CPU
0	1	1	0	Control word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

It is necessary to execute a function-setting sequence after resetting on MSM82C51A. Fig. 1 shows the function-setting sequence.

If the function was set, the device is ready to receive a command, thus enabling the transfer of data

by setting a necessary command, reading a status and reading/writing data.

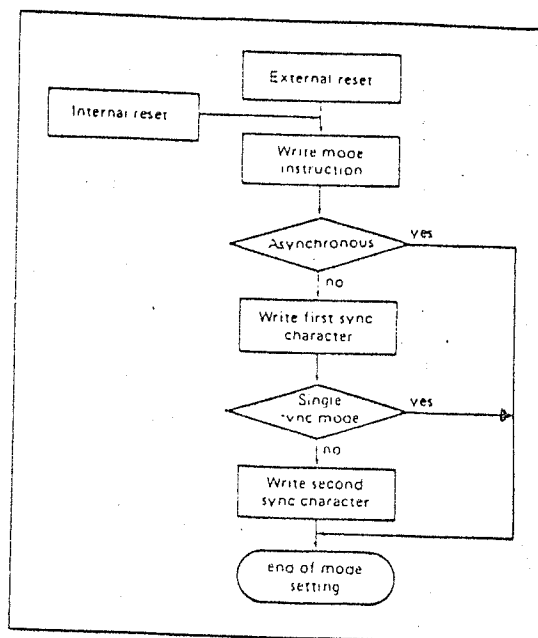


Fig. 1 Function-Setting Sequence (Mode Instruction Sequence)

Control Words

There are two types of control word.

1. Mode instruction (setting of function)
2. Command (setting of operation)

1) Mode Instruction

Mode instruction is used for setting the function of MSMB2C51A. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of control word after resetting will be recognized as "mode instruction."

Items to be set by mode instruction are as follows:

- Synchronous/asynchronous mode

- Stop bit length (asynchronous mode)
- Character length
- Parity bit
- Baud rate factor (asynchronous mode)
- Internal/external synchronization (synchronous mode)
- No. of synchronous characters (synchronous mode)

The bit configuration of mode instruction is shown in Fig. 2 and 3. In the case of synchronous mode, it is necessary to write one- or two-byte sync characters.

If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

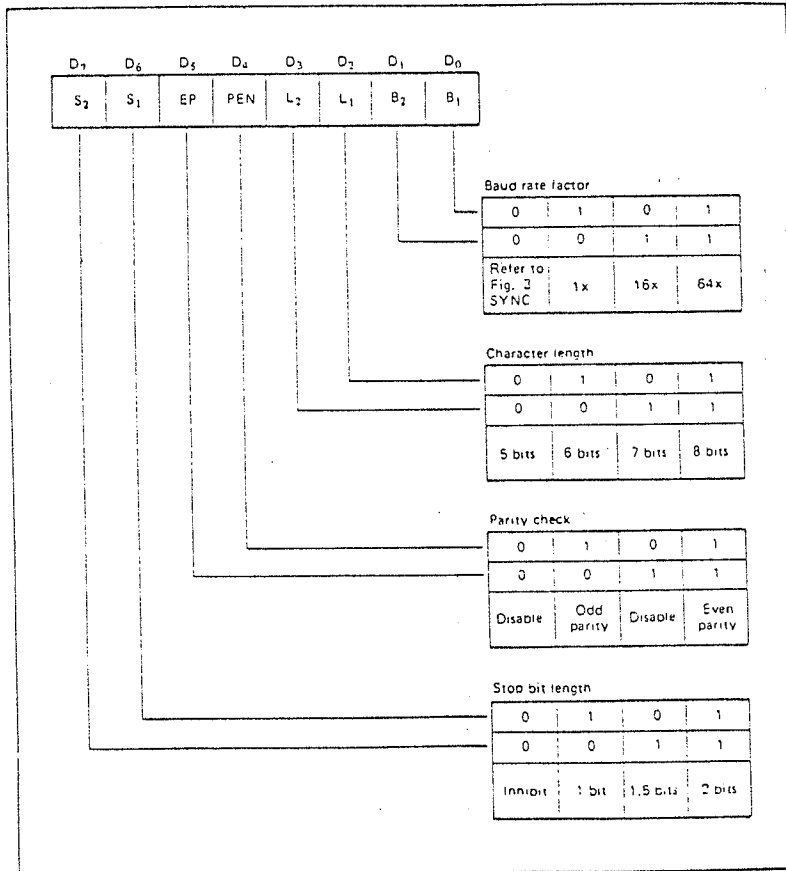


Fig. 2 Bit Configuration of Mode Instruction (Asynchronous)

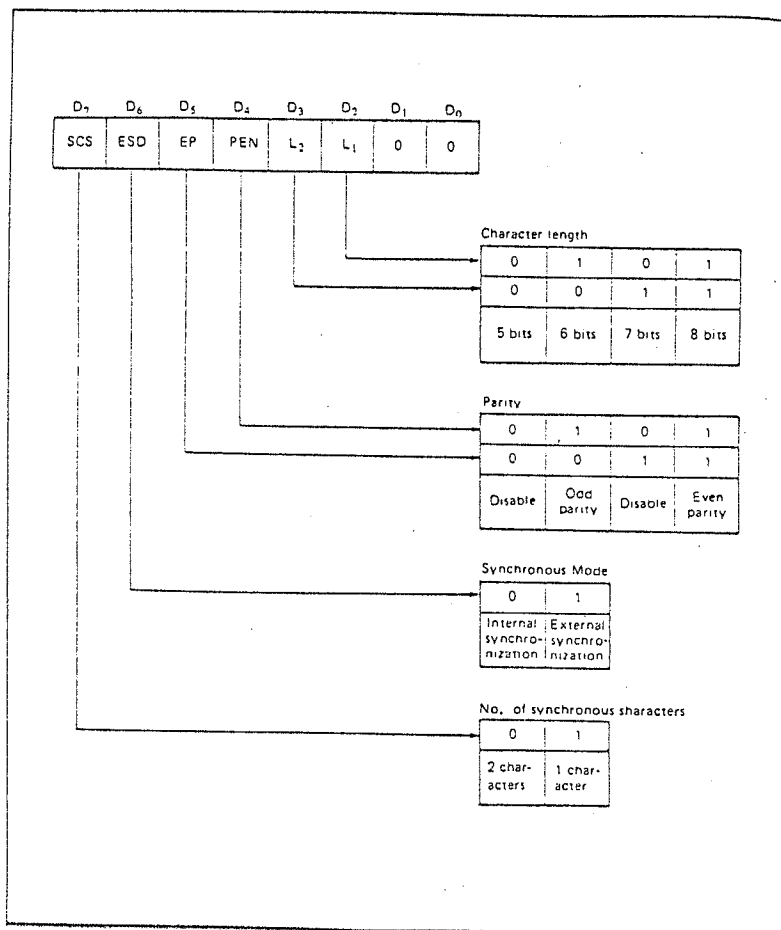


Fig. 3 Bit Configuration of Mode Instruction (Synchronous)

2) Command

Command is used for setting the operation of MSM82C51A.

It is possible to write a command whenever necessary after writing mode instruction and sync characters.

Items to be set by command are as follows:

- Transmit Enable/Disable

- Receive Enable/Disable
- \overline{DTR} , \overline{RTS} Output of data.
- Resetting of error flag.
- Sending of break characters
- Internal resetting
- Hunt mode (synchronous mode)

The bit configuration of a command is shown in Fig. 4.

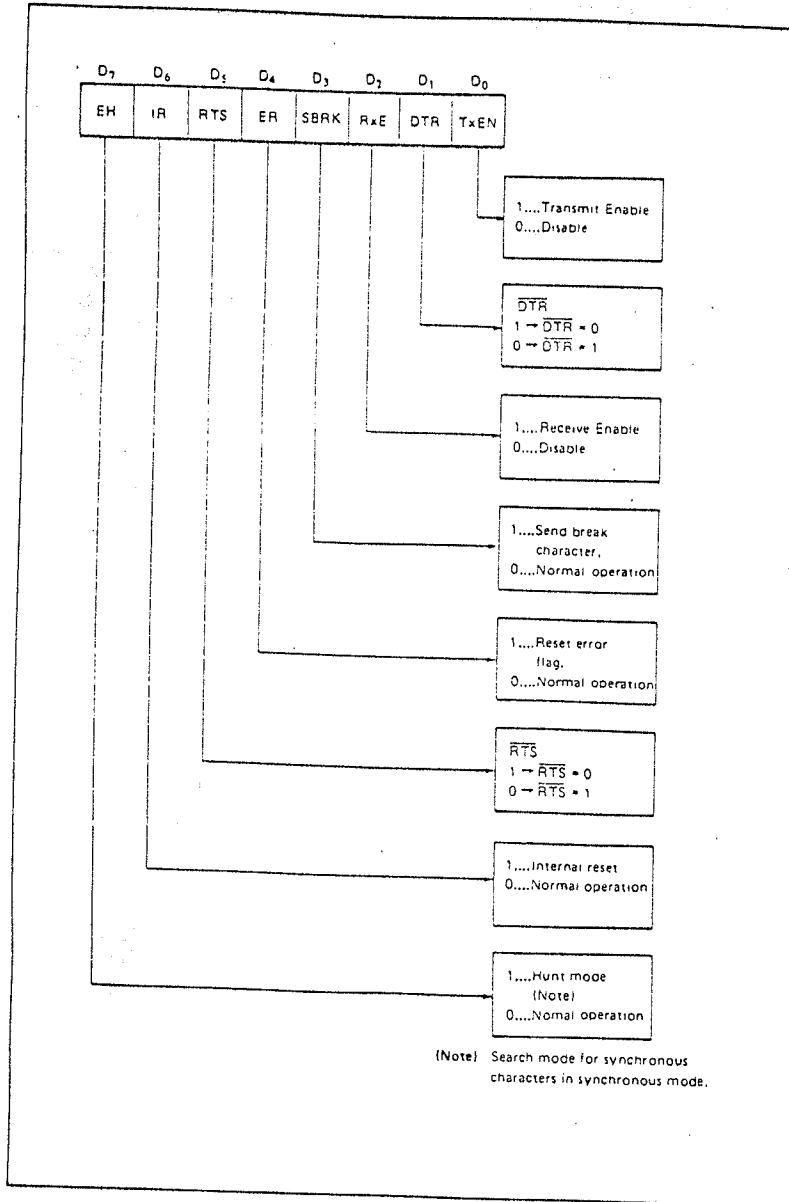


Fig. 4 Bit Configuration of Command

Standby Status

It is possible to put MSM82C51A in "standby status" for the complete static configuration of CMOS.

It is when the following conditions have been satisfied that MSM82C51A is in "standby status."

- (1) \overline{CS} terminal shall be fixed at Vcc level.
- (2) Input pins other than \overline{CS} , D₀ to D₇, \overline{RD} , \overline{WR} and $\overline{C/D}$ shall be fixed at Vcc or GND level (including SYNDT in external synchronous mode).

Note When all outputs current are 0, ICCS specification is applied.

4.4 MSM6255 LCD CONTROLLER

The following is the full list of the control code and instruction register of the MSM6255.

(1) Mode control

By writing "00H" in the instruction register, the mode control register can be assigned.

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	Read-able
Instruction register	1	0	0	0	0	0	0	0	0	
Mode control register	0	0	MODE DATA							

D6	D5	D4	D3	D2	D1	D0	Output system							
I/O	I/O	I/O	I/O	0	0	0	Normal	1-bit serial	Character display					
				1	0		ODD/EVEN							
				x	1		4-bit parallel							
				x	1		4-bit parallel							
				I/O	I/O	I/O	I/O	0		0	0	Normal	1-bit serial	Graphics
								1		0		ODD/EVEN		
								x		1		4-bit parallel		
								x		1		4-bit parallel		
Blinking time	Cursor ON/OFF	Cursor blinking	Display ON/OFF	ODD/EVEN	4-bit parallel/ 1-bit serial	Mode								

1: Display ON
0: Display OFF

D5 D4
0 0 Cursor OFF
0 1 Cursor OFF
1 0 Cursor ON
1 1 Cursor blinking

1: 16 frames
0: 32 frames } Half of blinking frequency

(2) Character pitch setting

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	0	0	0	1	Read-able
Character pitch register	0	$(V_p - 1)$				0	$(H_p - 1)$			Read-able

H_p represents the number of bits indicated in one byte indication data sent from RAM. The value of H_p is the following five types.

H_p	D2	D1	D0	
4	0	1	1	Horizontal character pitch 4
5	1	0	0	" 5
6	1	0	1	" 6
7	1	1	0	" 7
8	1	1	1	" 8

(3) Character number setting (per line)

	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	0	0	1	0	
Character number register	0	0	$(H_z - 1)$							Read-able

Assuming the total dot number to the horizontal direction of the display is N_H ,

$$N_H = H_p \times H_N, \text{ where } H_N = 2 \text{ to } 128.$$

The maximum value of $N_H = 8 \times 128 = 1,024$ dots.

(4) Time sharing number setting (display duty)

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	0	0	1	1	Read-able
Time sharing register	0	$(N_x - 1)$								

$$N_x = 1 \text{ to } 256$$

(5) Cursor shape setting

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	0	1	0	1	Read-able
Cursor position register	0	$(C_{pu} - 1)$				$(C_{pd} - 1)$				Read-able

In the character display (character mode), on lines from C_{pu} to C_{pd} , the cursor is indicated. For example, when $C_{pu} = C_{pd} = 8$ is specified while 5 x 7 dot font is used, the cursor is displayed below a character.

The length of the cursor to the horizontal direction becomes the same as the character pitch to the horizontal direction: H_p . If $C_{pu}, C_{pd} \leq V_p$, the cursor is indicated with the highest priority. whereas, $C_{pu}, C_{pd} > V_p$, the cursor is not indicated. This setting is invalid in the graphic mode.

(6) Display start lower address setting

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	0	1	0	1	Read-able
Indication start address register (lower byte)	0	Lower start address								Read-able

(7) Display start upper address setting

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	0	1	1	0	Read-able
Indication start address register (upper byte)	0	Upper start address								Read-able

The display start address shows an address of the RAM which stores data indicated at the left end and the most upper position. The start address is composed of upper and lower 8 bits (16 bits in total) in the graphic mode. In the character display mode, it is composed of the lower 6 bits (D5 to D0) of the upper address and the lower 8 bits (14 bits in total). In the case, the upper 2 bits of the upper address are ignored.

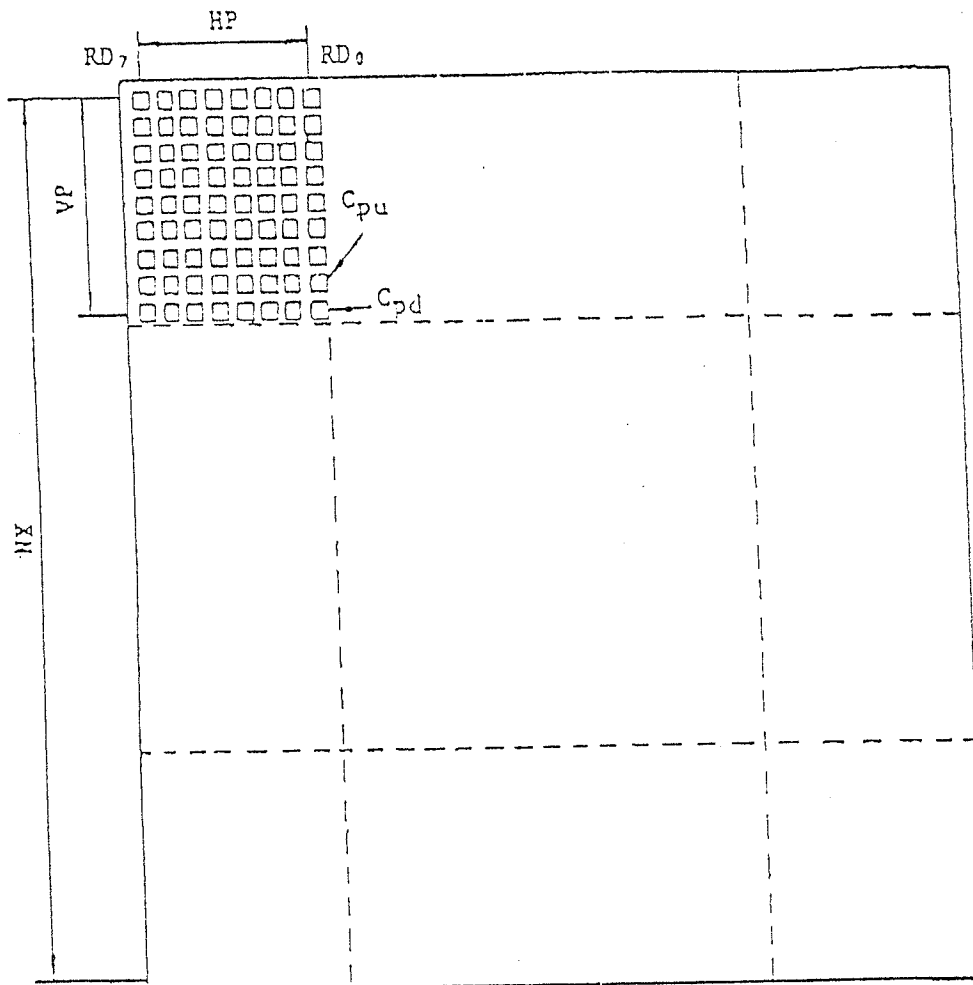
(8) Cursor's lower address setting

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	0	1	1	1	Read-able
Cursor address register (lower byte)	0	(Lower cursor address)								

(9) Cursor's address setting

Register	A0	D7	D6	D5	D4	D3	D2	D1	D0	
Instruction register	1	0	0	0	0	1	0	0	0	Read-able
Cursor address register (upper byte)	0	(Upper cursor address)								Read-able

By means of this instruction, the value of the cursor address is written in the cursor address register. In the graphic mode, the cursor is indicated at the position specified by the cursor address register.



Symbol	Name	Meaning	Value
Hp	Horizontal character pitch	Pitch of character to the horizontal direction	6 to 8 dots
H_N	Horizontal character number	Number of characters/words per line	2 to 128 characters
Vp	Vertical character pitch	Pitch of character to the vertical direction	1 to 16 dots
Cpu	Cursor start position	A position where the cursor starts display	1 to 16 lines
Cpd	Cursor end position	A position where the cursor stops display	1 to 16 lines
N_X	Vertical direction line number	Display duty	1 to 256

CHAPTER 5

SPARE PARTS PRICE LIST

ORDER NO	DESCRIPTION	FOB HK (US\$)
IC04HC	IC 74HC04	0.30
IC04HCU	IC 74HCU04	0.30
IC08HC	IC 74HC08	0.30
IC138HC	IC 74HC138	0.50
IC1488	IC 1488	0.40
IC1489	IC 1489	0.40
IC157HC	IC 74HC157	0.50
IC161HC	IC 74HC161	0.60
IC245HC	IC 74HC245	1.10
IC273HC	IC 74HC273	0.90
IC2797	FLOPPY DISK CONTROLLER	9.50
IC32HC	IC 74HC32	0.30
IC6255	MSM6255GS LCD CONTROLLER	9.40
IC74HC	IC 74HC74	0.40
IC80L	LOW POWER Z80L CPU 2.5MH	5.20
IC82C51	MSM 82C51ARS USART	2.60
IC82C53	MSM82C53-5RS TIMER	2.60
IC82C55	MSM82C55A-5RS PPI	2.60
IL07	IC 7407	0.30
IL14LS	IC 74LS14	0.20
IL38LS	IC 74LS38	0.20
IL45	IC 7445	0.50
IM2732-45	IC2732 EPROM 450NS	2.40
IM416420	4164 D. RAM 200NS	0.60
IM611620	6116 STATIC RAM 200NS	1.80
MC32016	16MHZ X'TAL	0.50
SPBW0201-02	MAIN PBC VER 1.6	7.30
IA78L12	78L12 REGULATOR	0.30
IC555C	CMOS IC555	0.30
ICL296	ICL296 SWITCHING REGULAT	3.00
ICL8211	ICL8211 VOLT DESTESTOR	1.50
ICTL497AC	ICTL497AC SWITCHING RGLR	1.10
ID0006	IN5822 SWITCHING DIODE	0.50
IT0004	TRANSISTOR 9014B	0.10
IT0012	TRANSISTOR 9015B	0.10
MS023	5V REED RELAY SPST	1.00
RV2501H	5KOHM VR (H TYPE)	0.10
RV3201H	20K OHM VR (H TYPE)	0.10
SPBW0202-01	POWER PCB BOARD	0.30

DL003	2X5 LED RED	0.10
MP021-2	BW02 MALE ADAPTOR JACK	0.10
SPBW0203-01	KEYBOARD PCB	1.10
WN020001	CABINET TOP	2.20
WN020002	CABINET BOTTOM	2.20
WN020003	DISPLAY FRONT CABINET	0.50
WN020004	DISPLAY BACK CABINET	0.60
WN020005	HINGE	0.10
WN020006	HINGE PLASTIC BUSHING	0.10
WN020007	HANDLE	0.20
WN020008	I/O DOOR	0.10
WN020009	DISPLAY LOCK HOOK	0.10
WN020011	CARTRIDGE TOP	0.40
WN020017-1	BW2 MODULE LENS	1.10
YSBW0201	3.5" FLOPPY DISK DRIVE	86.00
YSBW0202	LCD MODULE CG640200G	123.40
YSBW0203	BATTERY 6V 3AH RECHARGE	5.30

Effective Date : 1st September, 1985.

CHAPTER 6 CIRCUIT SCHEMATIC AND COMPONENT LAYOUT

- Fig. A1 CPU & BOOT ROM
 A2 Refresh & I/O Logic
 A3 Dynamic RAM
 A4 VRAM & LCD Display
 A5 Parallel I/O & Floppy Disk Controller
 A6 Timer & Serial I/O
 A7 Power Board

- Fig. B1 Main PCB Component Layout
 B2 PCB Layout, Component Side
 B3 PCB Layout, Solder Side
 B4 Power Board Component & PCB Layout

- Fig. C1 Connector Schematic Diagram
 C2 Inter-Board Connector Diagram
 C3 Inter-Board Connector Table

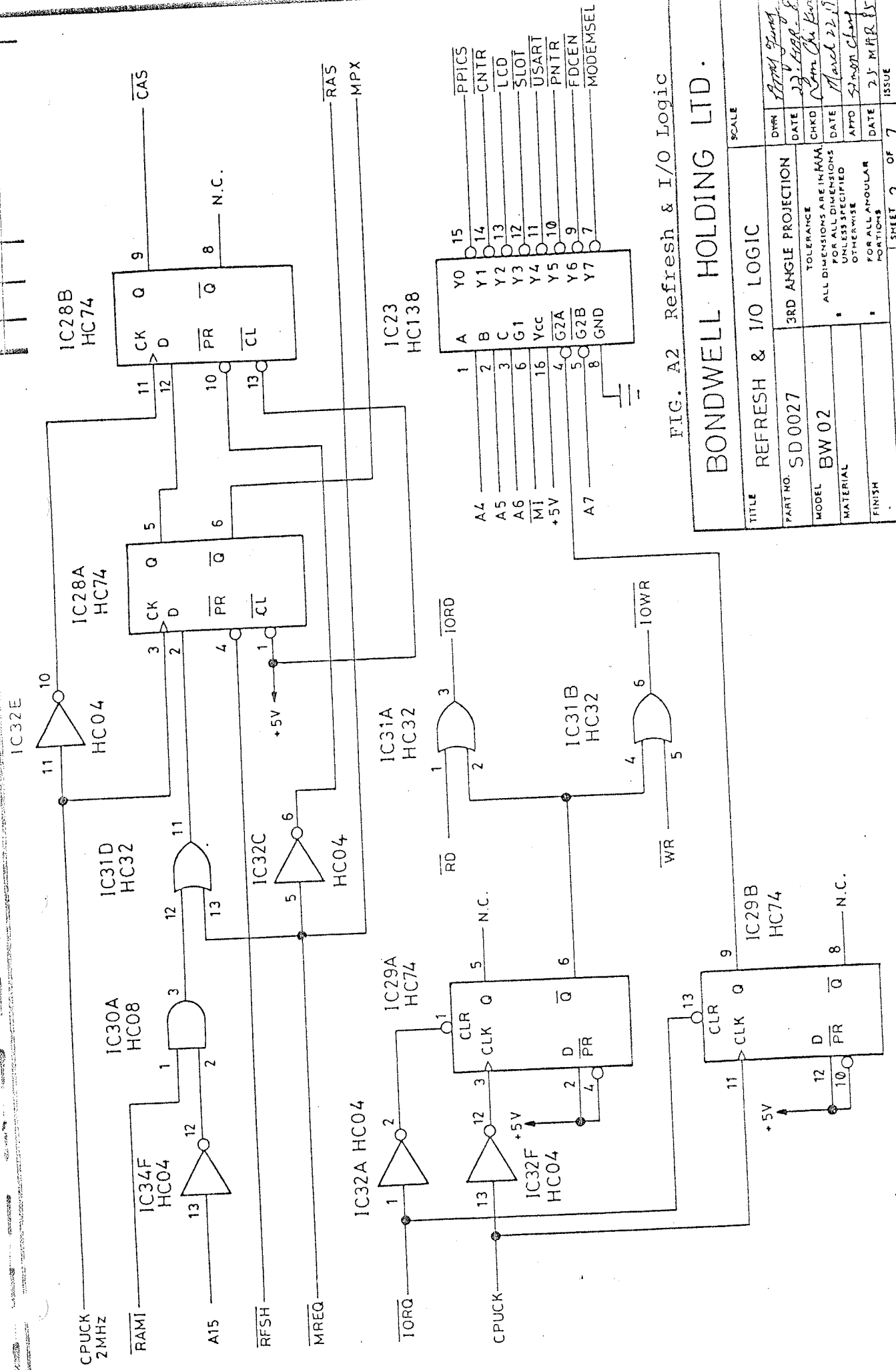
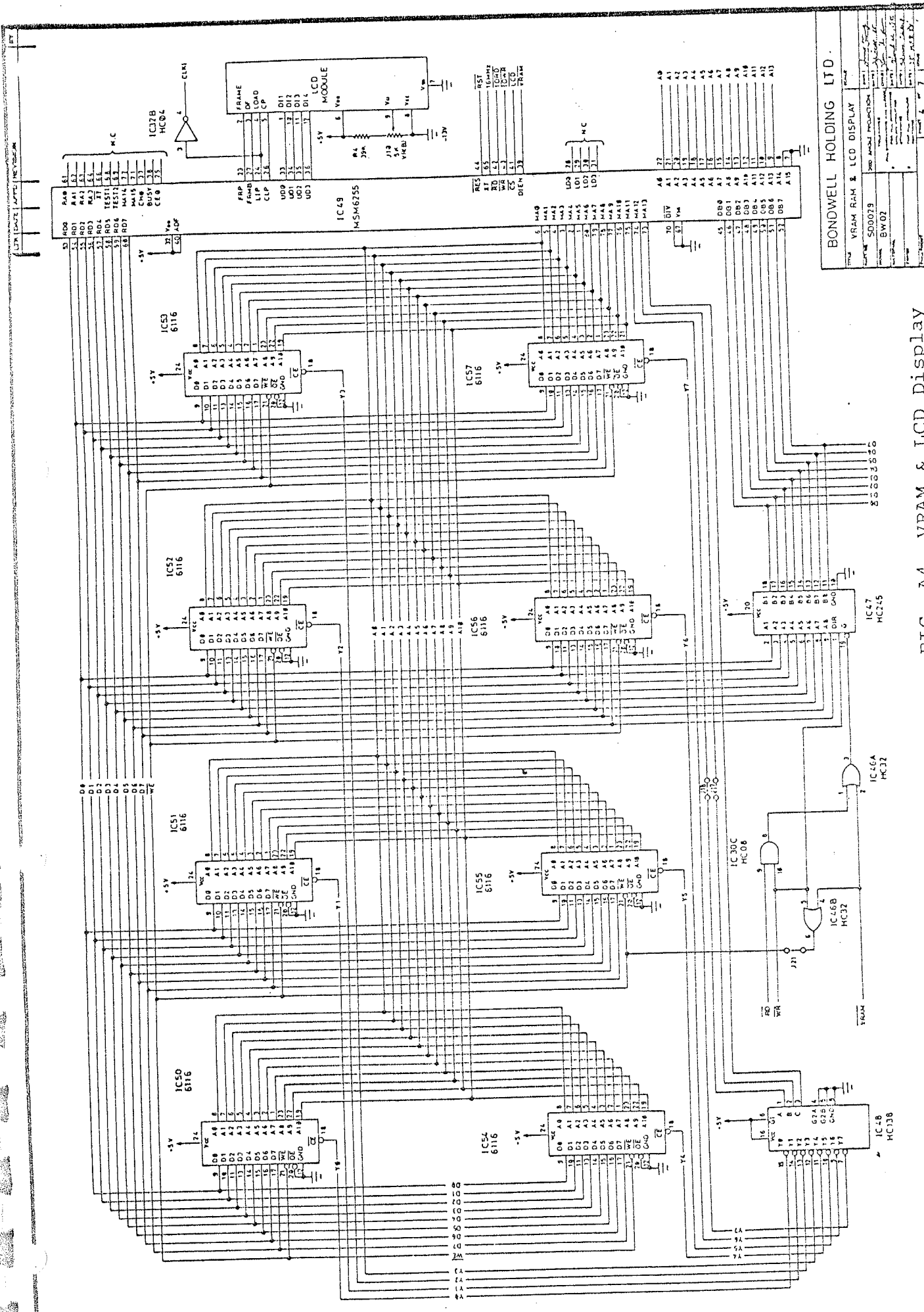


FIG. A2 Refresh & I/O Logic

BONDWELL HOLDING LTD.

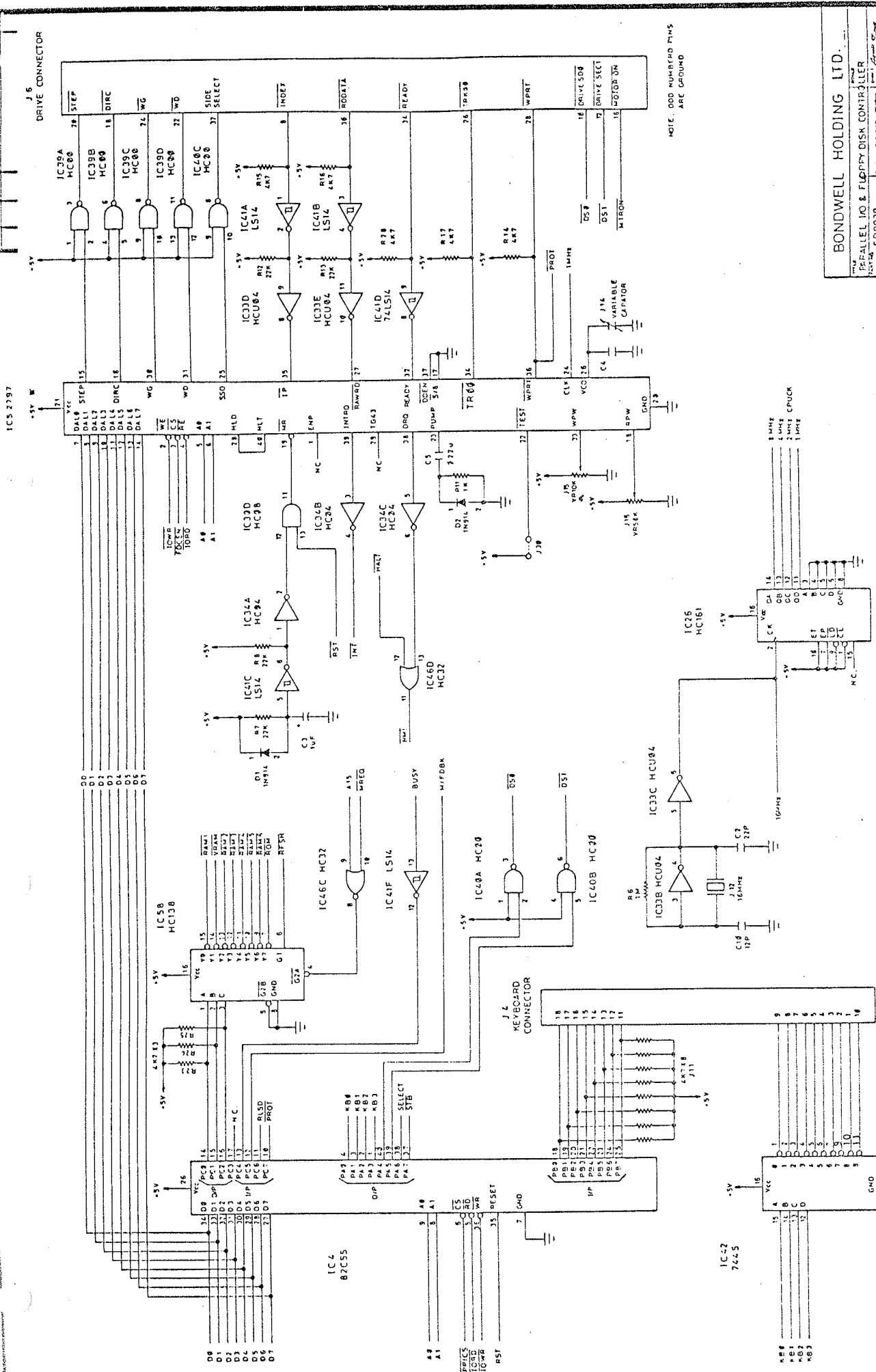
TITLE	REFRESH & I/O LOGIC	SCALE	
PART NO.	SD 0027	3RD ANGLE PROJECTION	
MODEL	BW 02	TOLERANCE	
MATERIAL		FOR ALL DIMENSIONS	
FINISH		UNLESS SPECIFIED	
TREATMENT		FOR ALL APPLICABLE	
		PORTIONS	
		SHEET 2	OF 7
DWR	<i>Shyam Singh</i>	DATE	<i>22.11.85</i>
CHKD	<i>Manoj Kumar</i>	DATE	<i>22.11.85</i>
APD	<i>Manoj Kumar</i>	DATE	<i>22.11.85</i>
ISSUE		DATE	<i>25.11.85</i>



BONDWELL HOLDING LTD.

VRAM RAM & LCD DISPLAY
SD0009
SW02
REV. 1
DATE: 1988.12.15
DESIGNER: [Name]
CHECKER: [Name]
APPROVER: [Name]
DATE: 1988.12.15

FIG. A4 VRAM & LCD Display



NOTE: 000 NUMBERED PINS ARE GROUND

BONDWELL HOLDING LTD.

PARALLEL I/O & FLOPPY DISK CONTROLLER

500030

BW02

DATE: 1982.05.10

DESIGNER: [Signature]

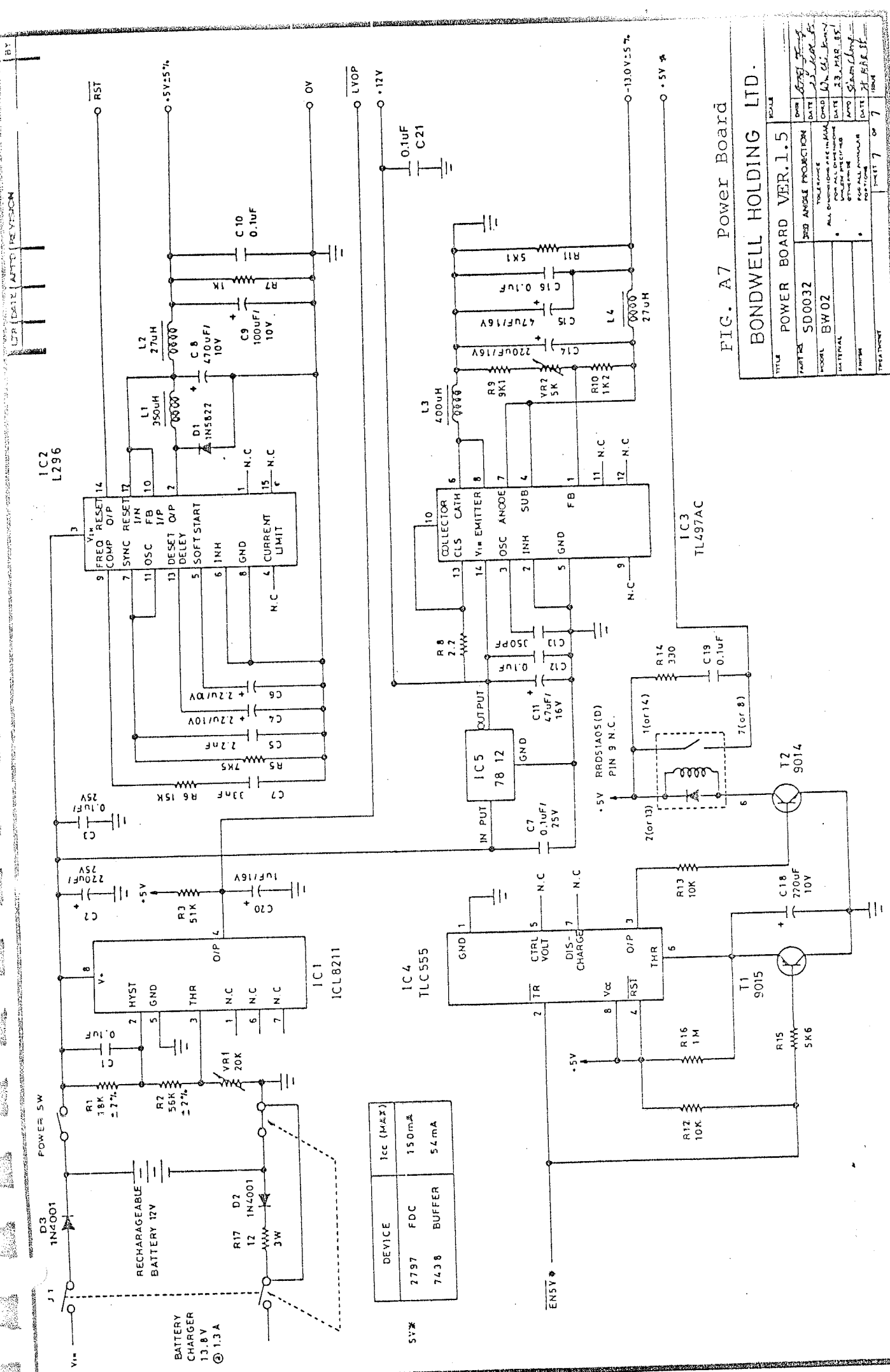
CHECKED: [Signature]

APPROVED: [Signature]

PROJECT: [Signature]

REV: 5

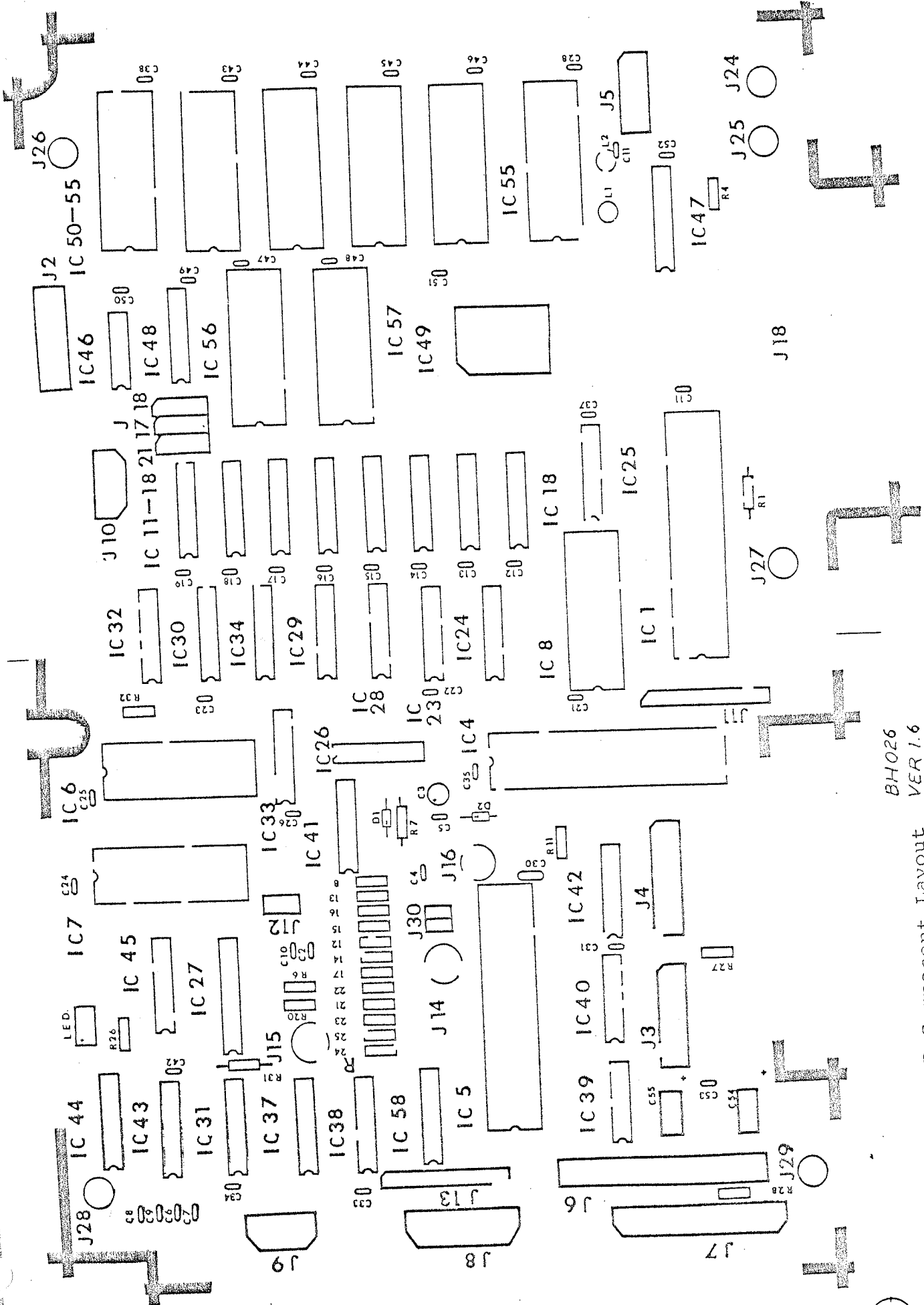
FIG. A5 Parallel I/O & Floppy Disk Controller



DEVICE	I _{CC} (MAX)
7797	FDC 150mA
7438	BUFFER 54mA

FIG. A7 Power Board

TITLE		ISSUE	
POWER BOARD VER.1.5		DATE	BY
PART NO. SD0032		DATE	BY
MODEL NO. BW02		DATE	BY
DESIGNED BY		DATE	BY
CHECKED BY		DATE	BY
DRAWN BY		DATE	BY
APPROVED BY		DATE	BY
PAGE NO.		PAGE TOTAL	
SHEET 7		OF 7	



BH026
VER 1.6

FIG. B1 Main PCB Component Layout

DESIGNED BY: LAM CHI KUAN

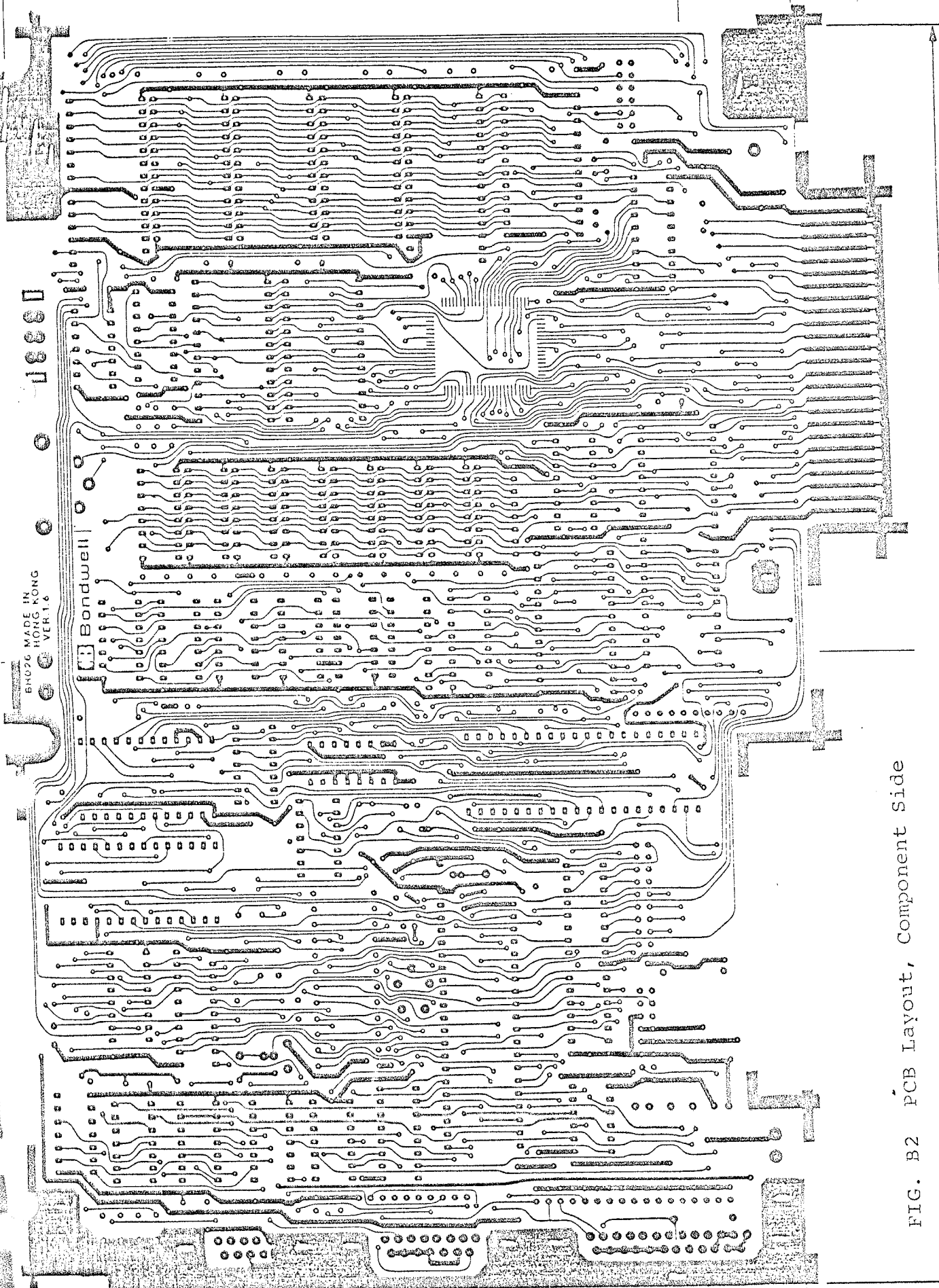
REDUCE TO 166.5



1888

BONDWELL MADE IN HONG KONG VERT. 6

Bondwell

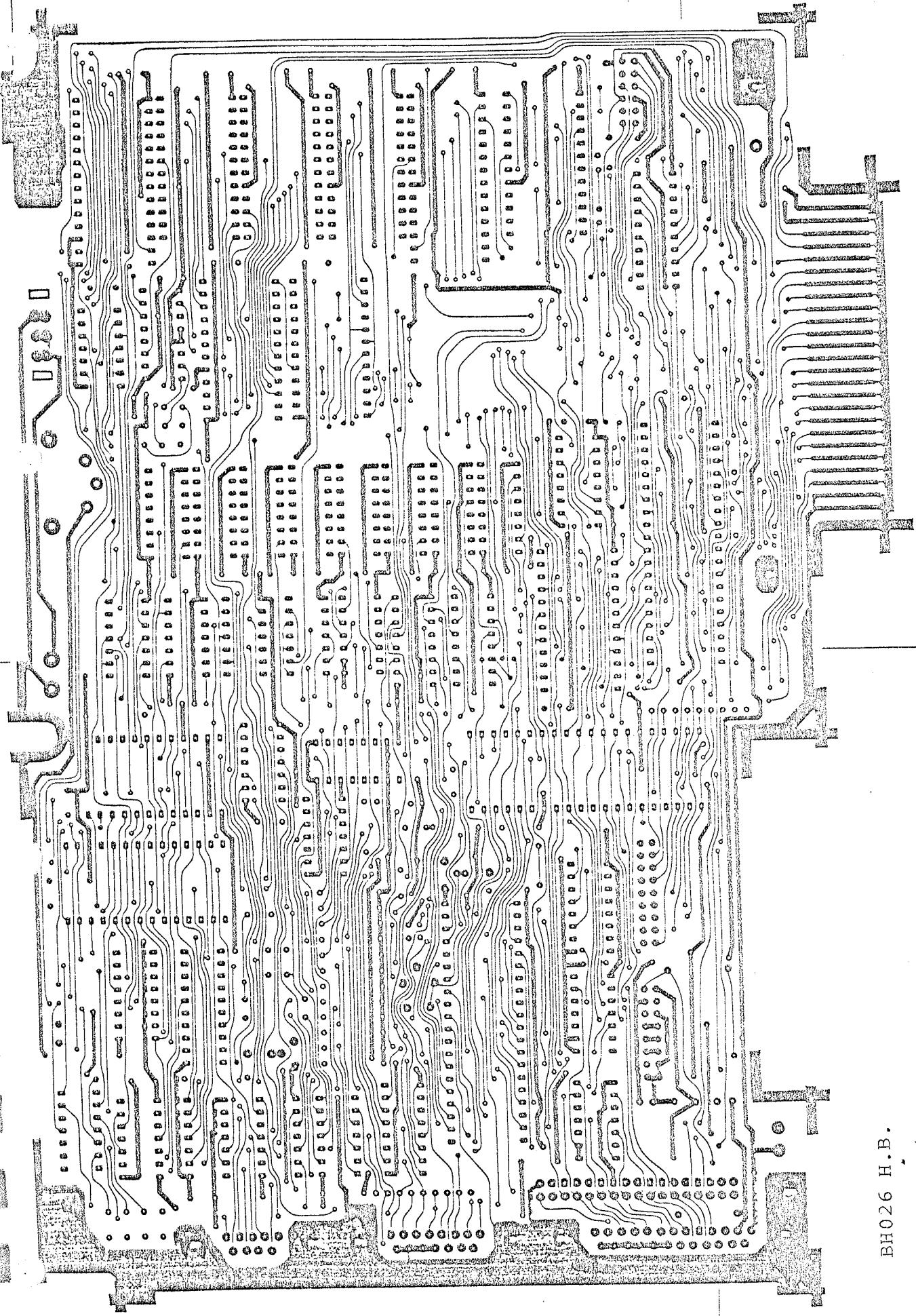


254 mm.

FIG. B2 PCB Layout, Component Side

Drawn by: LIM CHI KUAN

REDUCE TO 166.5



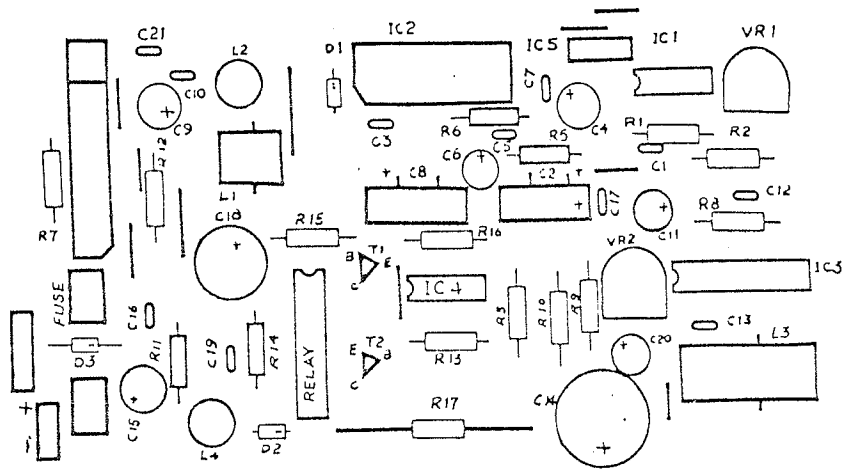
BH026 H.B.

FIG. B3 PCB Layout, Solder Side

DRAWN BY: LPM CHL RMAN



DESIGN BY: LAM CHI KUAN



BH026 POWER BOARD
VER 1.5

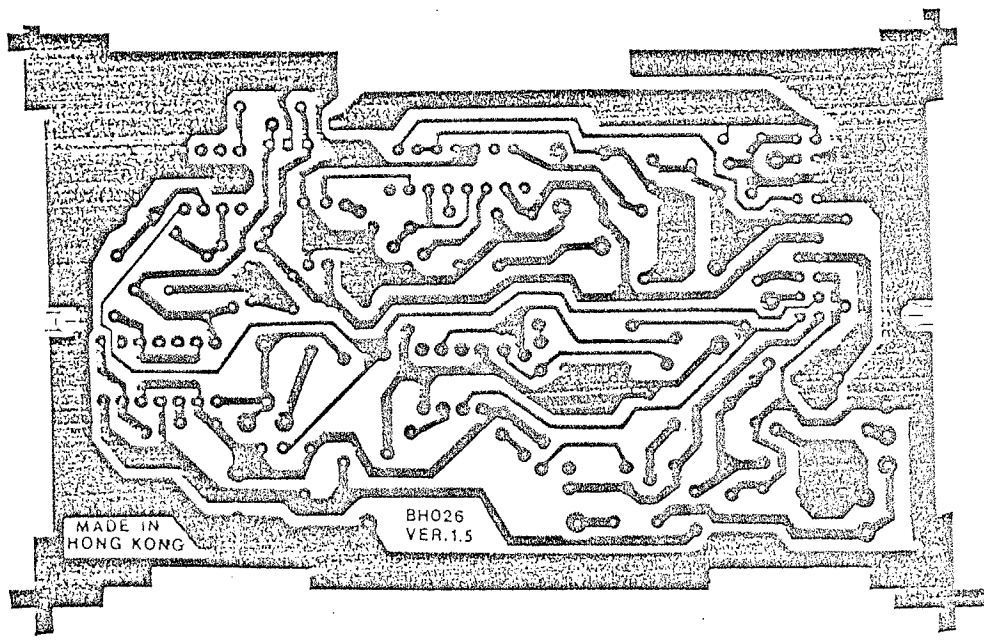
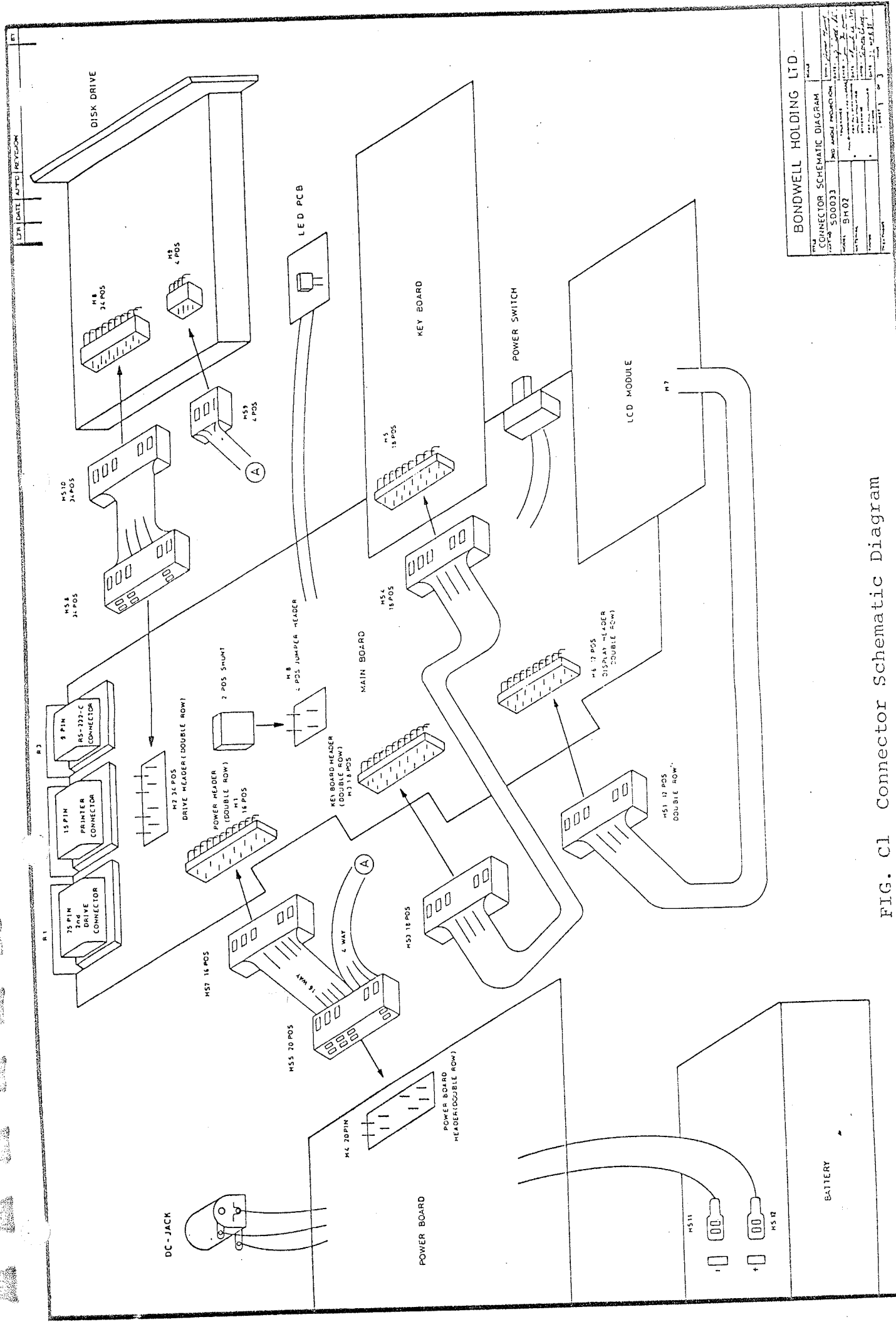


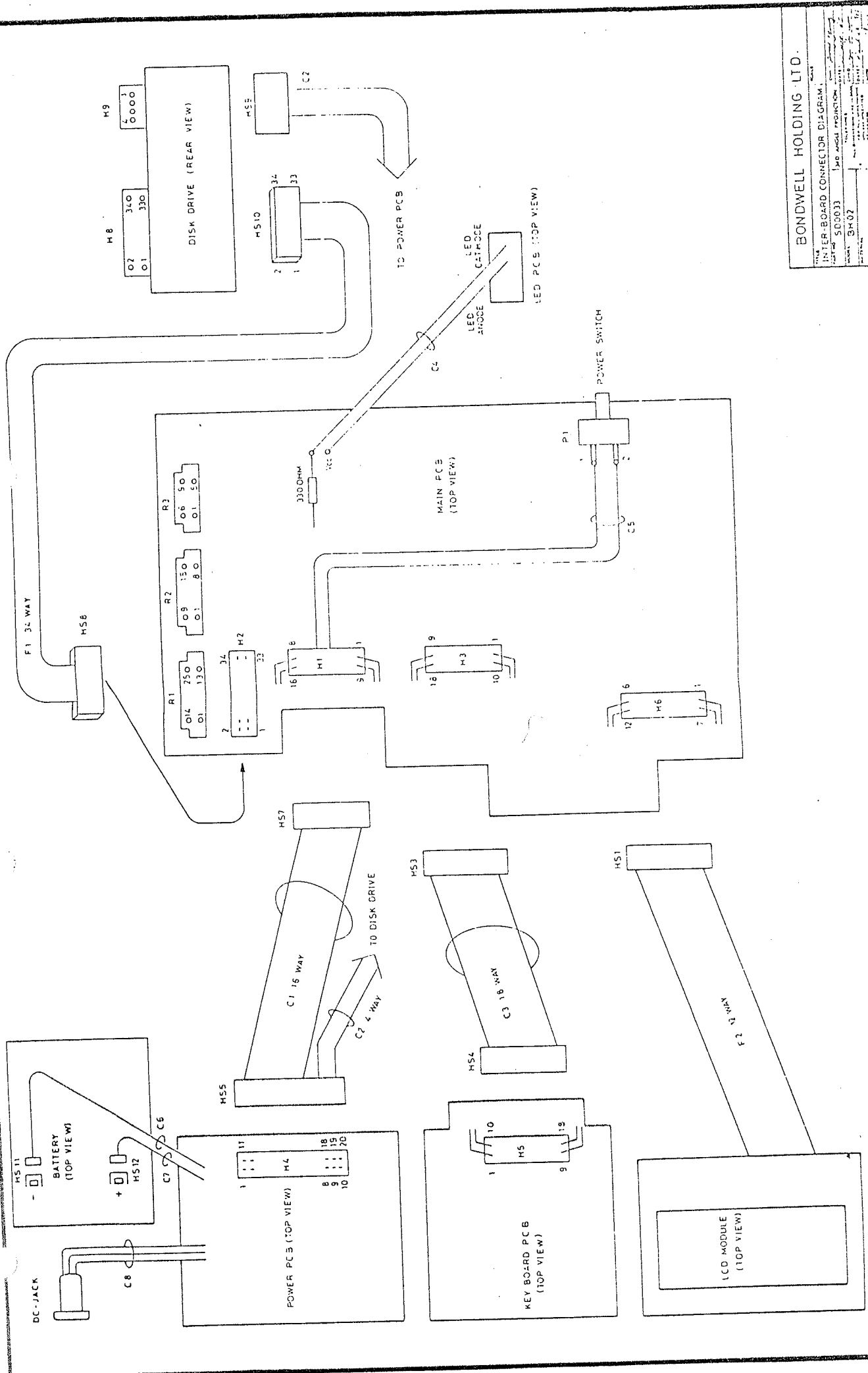
FIG. B4 Power Board Component & PCB Layout



BONDWELL HOLDING LTD.	
PCB CONNECTOR SCHEMATIC DIAGRAM	DATE: 1988.08.10
PROJECT: BH02	DESIGNER: CHEN
DATE: 1988.08.10	CHECKER: CHEN
DATE: 1988.08.10	APPROVER: CHEN
DATE: 1988.08.10	DATE: 1988.08.10

FIG. C1 Connector Schematic Diagram

DESIGN BY: LAM CHI KUAN



BONDWELL HOLDING LTD.

INTER-BOARD CONNECTOR DIAGRAM	DATE
DATE 500033	JOB NO. 500033
DESIGNER 94102	DESIGNER
CHECKER	CHECKER
APPROVER	APPROVER
DATE	DATE
SCALE	SCALE
FIG. NO. 7	FIG. NO. 7

FIG. C2 Inter-Board Connector Diagram

RAM CARD for BW2 v.1.0

H4 PIN NO.	H1 PIN NO.	H9 PIN NO.	SIGNAL
1	1		ENVSV *
2	2		-12V
3	3		5V
4	4		J1
5	5		12V
6	6		5V
7	7		RST
8	8		GND
9		1	5V
10		7	GND
11	9		5V #
12	10		LYOP
13	11		GND
14	12		J1
15	13		12V
16	14		5V
17	15		GND
18	16		GND
19		3	GND
20		4	12V

H3 PIN NO.	H5 PIN NO.	SIGNAL
1	1	OUT 8
2	2	OUT 7
3	3	OUT 6
4	4	OUT 5
5	5	OUT 4
6	6	OUT 3
7	7	OUT 2
8	8	OUT 1
9	9	OUT 0
10	10	OUT 9
11	11	PB7
12	12	PB6
13	13	PB5
14	14	PB4
15	15	PB3
16	16	PB2
17	17	PB1
18	18	PB 0

H6 PIN NO.	H7 PIN NO.	SIGNAL
1	6	-5V
2	4	LIP
3	2	FRP
4	7	GND
5	9	V0
6	11	UD2
7	5	CLP
8	3	FRMB
9	1	UD 0
10	8	-12V
11	10	UD1
12	12	UD3

- HS1 12 POSITION HOUSING DOUBLE ROW
- HS3 18 POSITION HOUSING DOUBLE ROW
- HS4 18 POSITION HOUSING DOUBLE ROW
- HS5 20 POSITION HOUSING DOUBLE ROW
- HS7 16 POSITION HOUSING DOUBLE ROW
- HS8 34 POSITION FLAT CABLE CONNECTOR
- HS10 34 POSITION FLAT CABLE CONNECTOR
- HS9 4 POSITION HOUSING SINGLE ROW
- HS11 TERMINEL RECEPTACLE
- HS12 TERMINEL RECEPTACLE

BONDWELL HOLDING LTD.

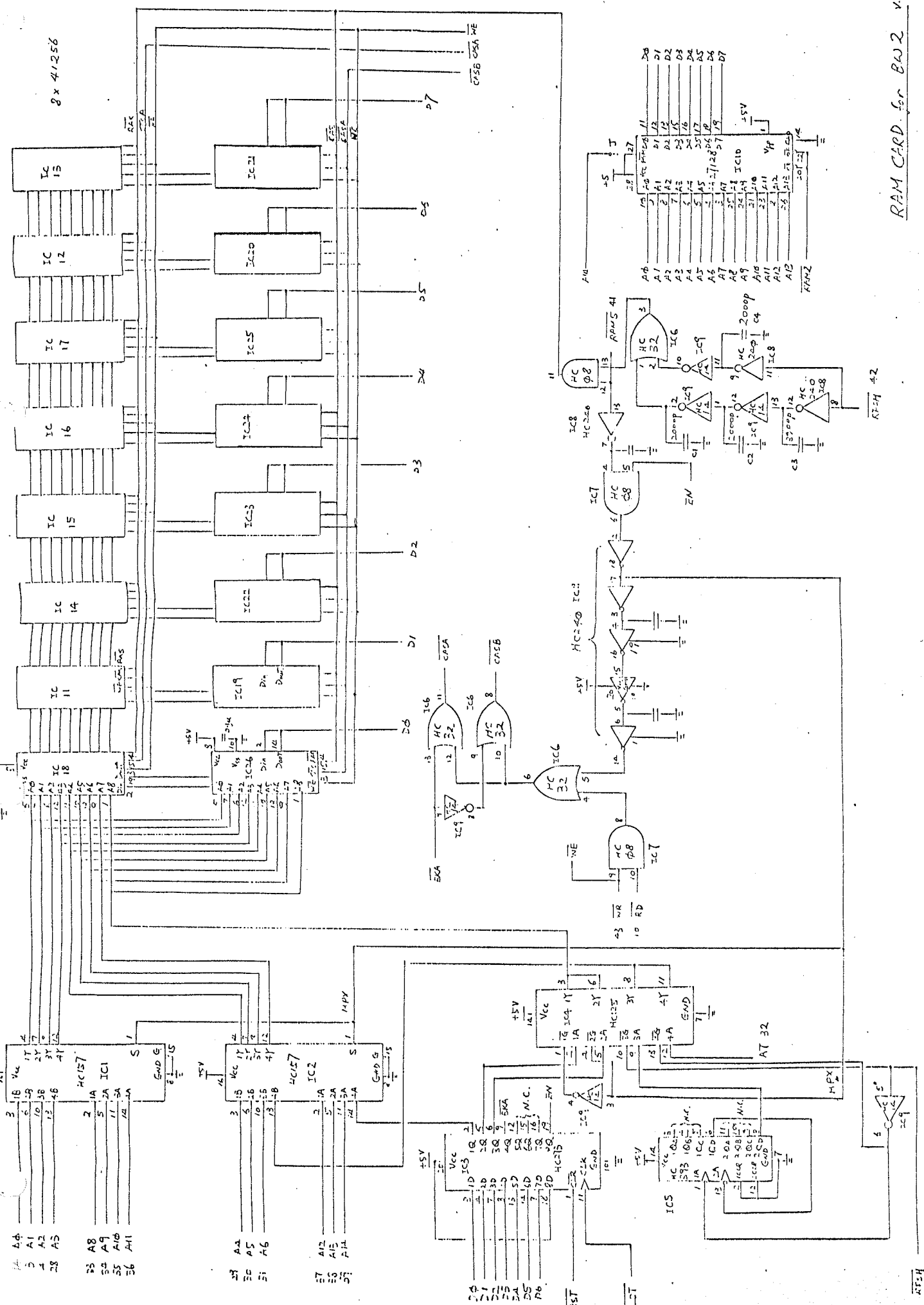
TITLE: INTER-BOARD CONNECTION TABLE		SCALE:
PART NO: SD0035		3RD ANGLE PROJECTION
MODEL: BH02	TOLERANCE:	DATE: 23 MAR 51
MATERIAL:	FOR ALL DIMENSIONS:	DATE: 23 MAR 51
FINISH:	UNLESS OTHERWISE SPECIFIED:	DATE: 23 MAR 51
PREPARED:	APPROVED:	DATE: 23 MAR 51
SHEET 3 OF 3		ISSUE

FIG. C3 Inter-Board Connector Table

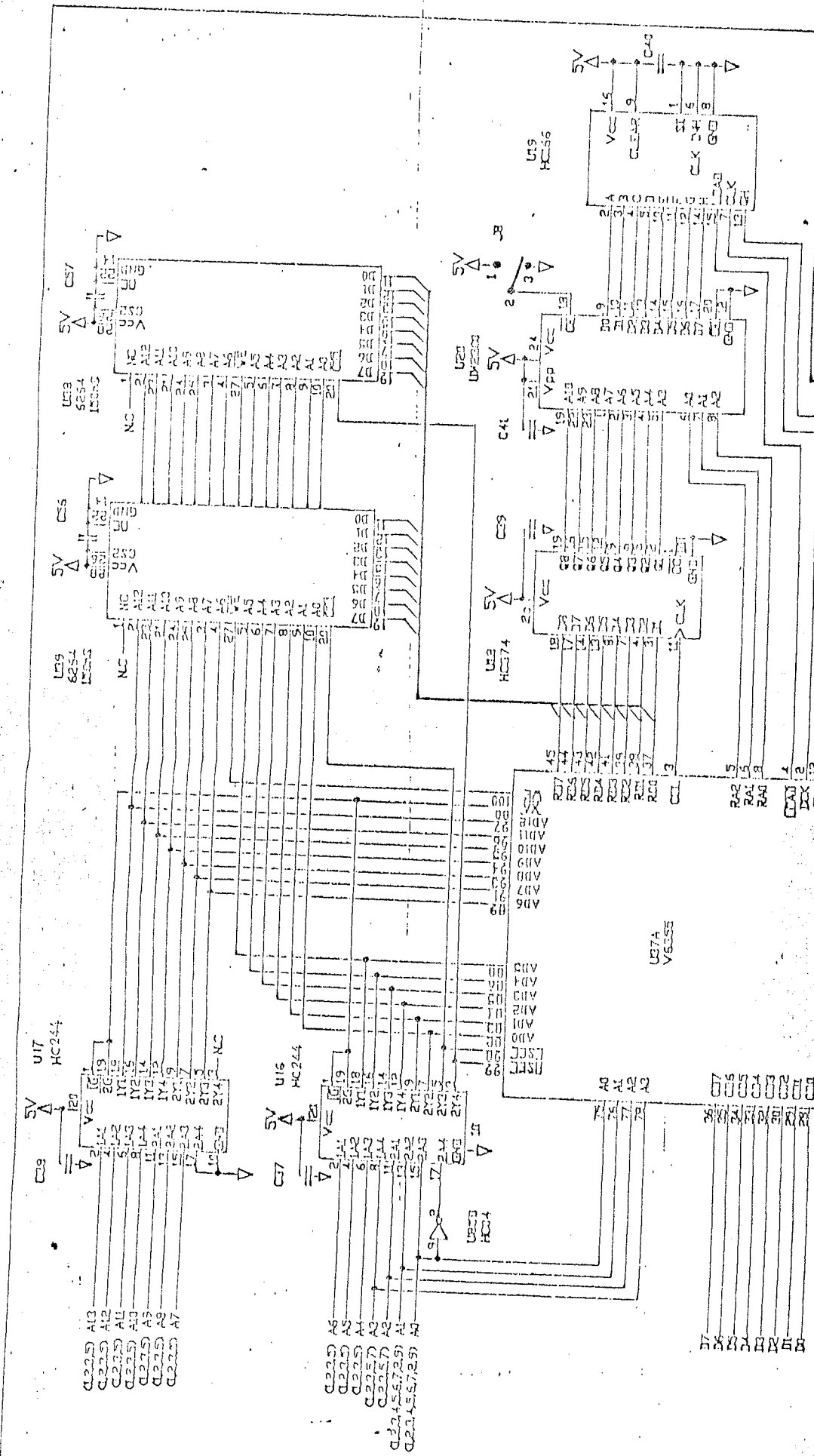
RAM CARD for BW2 v.1.0

15V
 47µF
 16V

8 x 41256

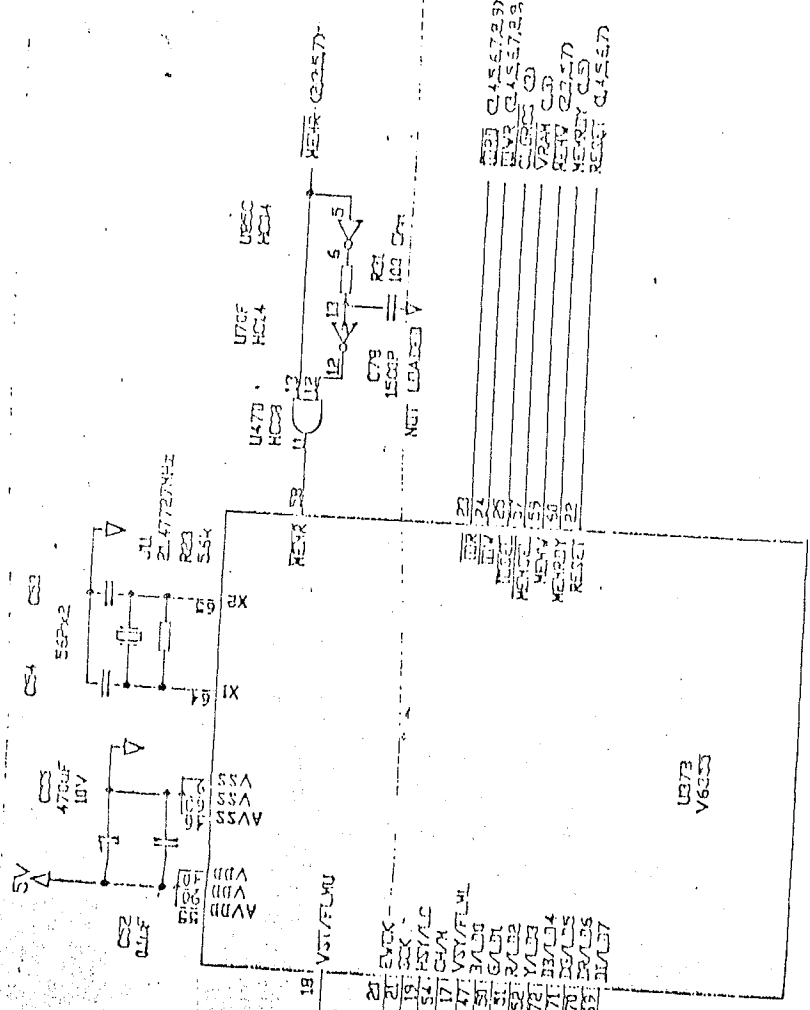
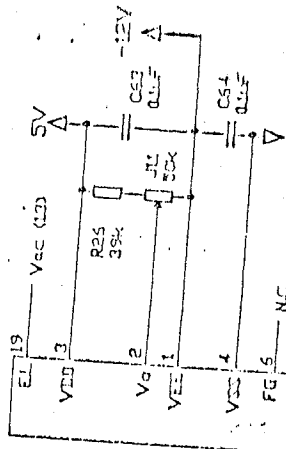


RAM CARD for BW2 v.1.0
 DAFAN BY: LAM CHI KUAN



BONDWELL HOLDING LTD.			
TITLE: VIDEO CONTROLLER (A)	CHKD: C.K. Lam	DATE: 17/11/75	DATE: 21/12/75
MODEL: 608	DATE: 1/1	APPD: C.K. Lam	DATE: 21/12/75
REV: 1/1	DATE: 17/11/75	DATE: 21/12/75	SHEET 10 OF 13
DRAWN: S. Chan	DATE: 17/11/75	DATE: 21/12/75	
PART NO.			

J15
20 WAYS
LCD HEADER



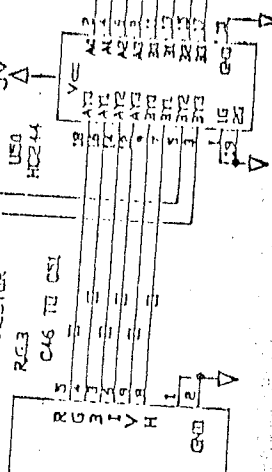
- U473 (HCO9) Q156729
- U70F (HCL4) Q156729
- U85C (HCL4) Q156729
- R20 (100) Q156729
- R21 (100) Q156729
- R22 (100) Q156729
- R23 (100) Q156729
- R24 (100) Q156729
- R25 (39K) Q156729
- R26 (100) Q156729
- R27 (100) Q156729
- R28 (100) Q156729
- R29 (100) Q156729
- R30 (100) Q156729
- R31 (100) Q156729
- R32 (100) Q156729
- R33 (100) Q156729
- R34 (100) Q156729
- R35 (100) Q156729
- R36 (100) Q156729
- R37 (100) Q156729
- R38 (100) Q156729
- R39 (100) Q156729
- R40 (100) Q156729
- R41 (100) Q156729
- R42 (100) Q156729
- R43 (100) Q156729
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- R94 (100) Q156729
- R95 (100) Q156729
- R96 (100) Q156729
- R97 (100) Q156729
- R98 (100) Q156729
- R99 (100) Q156729
- R100 (100) Q156729

NC [17410214, 1516, 25, 27, 29, 48, 49, 51, 52, 53, 54, 55, 56, 57, 62, 73, 74, 78, 80, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100]

BONDWELL HOLDING LTD.			
TITLE:	VIDEO CONTROLLER	(8)	
MODEL:	809	CHKD:	C.K. Lim
REV:	1-1	DATE:	15/2/86
DWN:	Sanson	APPD:	Simon Chan
DATE:	27 May 76	DATE:	20 MAY 81
PART NO.		SHEET	11 OF 15



J14
9 WAY D-TYPE
CONNECTOR



J20
COMPOSITE VIDEO DP

